TM 11-7010-200-10-9-2

TECHNICAL MANUAL

USERS MANUAL

COMMUNICATION PROCESSOR
MODEL IS/1000
TYPE AN/UYQ ( )

HEADQUARTERS, DEPARTMENT OF THE ARMY
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For explanation of abbreviations see, AR 310-50.

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SECTION 1
INTRODUCTION

1.1 PURPOSE

This technical manual describes the operation principles of, and gives application information for, the standard input/output (I/O) bus, the priority interrupt scheme and the direct-memory-access (DMA) feature used in the GTE/IS IS/1000 Communications Processor.

1.2 SCOPE

The information provided by this manual facilitates the design and programming of peripheral device controllers used in conjunction with the IS/1000 processor. As such, assumption is made that the person using this manual is skilled in state-of-the-art electronic and/or programming techniques, and has a thorough knowledge of solid-state computer logic implementation. A further requisite for the effective use of this manual is complete knowledge of the IS/1000 basic processor.

1.3 DOCUMENTATION

1.3.1 Publications

This manual supports all other manuals relating to the IS/1000 processor in general, but should be used specifically with the IS/1000 User's Manual, GTE/IS publication E0006.

1.3.2 Abbreviations and Conventions

Table 1-1 defines the abbreviations used in this publication. The following conventions are observed throughout the text:

- "$" preceding a number signifies that it is in hexadecimal notation.
- The names of instructions are capitalized for easy identification.
- Signal mnemonics that appear on logic diagrams and panel nomenclature are reproduced in all upper-case characters.
- TELEPRINTER MESSAGES ARE REPRODUCED IN 1403 TYPE STYLE, AS SHOWN IN THIS EXAMPLE.
- ONE and ZERO are used in text to represent binary "1" and binary "0" bit conditions, respectively.
- Values represented in teleprinter (TTY) messages by letters are reproduced in Scribe type style, as shown here.
- Relative signal polarity is indicated by a sign suffixed to the mnemonic. For example: PLXHFC- (more negative signal; approximately +0.2 Vdc), PLXHFC+ (more positive signal; approximately +3.7 Vdc).

Table 1-1. Abbreviations

Abbreviation	Meaning
A	Ampere.
dc	Direct current.
DMA	Direct memory access.
DTL	Diode-transistor logic.
ED	Expansion Distributor.
F	Farad.
GTE/IS	General Telephone and Electronics Information Systems, Inc.
HSPT	High-speed paper tape (reader).
Hz	Hertz.
IC	Integrated circuit.
I/O	Input/output.
IOP	I/O processor.
kHz	Kilohertz.
mA	Milliampere.
MHz	Megahertz.
mV	Millivolt.
ms	Millisecond.
ns	Nanosecond.
PC	Printed circuit.
pF	Picofarad.
Sync	Synchronization.
TTL	Transistor-transistor logic.
TTY	Teleprinter.
UCD	Utility Controller and Distributor.
us	Microsecond.
USASCII	United States of America Standard Code for Information Interchange.
Vac	Volts, alternating current.
Vdc	Volts, direct current.
XPM	Expanded Performance Module.

SECTION 2
DESCRIPTION

2.1 GENERAL

The interface provides a simple, standardized communication link through which information is exchanged within the IS/1000 processor system. The interface physically and electrically interconnects the processor, the memory, and various peripheral devices with their associated controllers. The channeling of information from one system entity to another is regulated by logically connecting and disconnecting the units according to a standardized set of logical conditions and timing criteria.

There are three types of interface operation:

1. The I/O bus, which channels information between the CPU and a peripheral device via the associated peripheral device controller.
2. The memory bus, which channels information between the CPU and the memory.
3. Direct memory access (DMA), which channels information between the memory and a peripheral device via the associated peripheral device controller.

2.1.1 I/O Bus

The I/O bus connects the CPU to a peripheral device via a suitable controller. The purpose of the controller is to provide compatibility between the operational requirements of the peripheral device(s) and the logical and electrical criteria of the CPU. Although GTE/IS provides several standard controllers, a custom controller can readily be designed by GTE/IS for the IS/1000 user due to the straightforward logic of the I/O bus.

With a controller connected to the I/O bus, communication between the CPU and the peripheral device is program controlled, either directly and entirely by the program, or in combination with the priority interrupt system.

2.1.1.1 Direct Program I/O Control

Although the use of interrupts is generally adopted in I/O control, it is possible to have the program start a peripheral device, then make a periodic check on the status of the controller until a ready condition is indicated. The program can then transfer data in word or block segments at the proper rate. Under direct program I/O control, the program must determine the correct rate of data exchange and monitor controller readiness.

2.1.1.2 Priority Interrupt I/O Control

Once a peripheral device has been started via its associated controller, the CPU can resume processing until the peripheral device

either has data for transmission or is ready to accept data. When the peripheral device requires servicing, the controller activates an interrupt line. The priority interrupt logic of the CPU causes the CPU to discontinue processing at the appropriate time to select and service the highest-priority interrupt pending. Data is transferred between the CPU and the controller during this interrupt service.

2.1.2 Memory Bus

The memory bus, which connects the memory directly to the CPU, is an asynchronous interface. Under normal circumstances, the memory does not supply data or accept a new address as fast as the CPU requires. Under these conditions, the CPU suspends processing until the memory is ready for the required function.

2.1.3 Direct Memory Access

The DMA channel enables direct data transfers between the memory and the I/O bus. Although the DMA channel physically utilizes the cable connections comprising the I/O bus and the memory interface, it bypasses the CPU logically. Each data transfer requires one memory cycle.

The DMA channel functions independently of the program since there are no instructions to affect it. To use the DMA channel, the processor must condition the peripheral device via the I/O bus, while the peripheral device requesting direct memory access, must supply the necessary control signals and address information to the memory. An Input/Output Processor (IOP), GTE/IS Model 4540-01, is optionally available to simplify use of the DMA channel. The IOP supplies signals and sequences the memory address for all standard peripheral devices.

2.1.4 General Specifications

The general specifications for the IS/1000 interface are listed in Table 2-1.

2.2 PHYSICAL DESCRIPTION

The signal interface consists of flat 50-conductor ribbon cables of various lengths, which plug onto the logic boards with dual-25 quick-connect press-on type edge connectors. The edge connectors terminate or branch off the cables so that one cable can have multiple connectors and interconnect several logic boards.

All interface logic is TTL implemented, using the latest MSI technology whenever possible. Each board contains its own driver/receiver logic for the signal lines that it uses. The logic implementing the priority interrupt system and the interrupt mask, is contained in the CPU assembly.

The cable line and connector pin numbering schemes are given in Figure 2-1.

Table 2-1. IS/1000 General Specifications

Characteristic	Specification
Functional	
Word Length	
Instruction	16 or 32 bits.
Data	16 bits.
Interrupts	
Internal	2 interrupts with separate priority levels (4 interrupts when an XPM option is used).
External	8 priority levels (expandable to 16 using an XPM option).
Electrical	
I/O Interface	
Standard	Shared by up to 64 addressable device controllers; data transfer rate up to 77,000 words per second (program dependent).
Logic Levels	
High	
TTL	+3.7 ± 1.7 V.
Low	
TTL	+0.2 ± 0.6 V.
Environmental	
Temperature	
Storage	-25° C to +75° C.
Operating	0° C to +55° C.
Humidity	0 to 90% relative without condensation.
Controller Circuitry	
Input (CPU to Controller)	TTL (Medium Speed recommended).
Output (Controller to CPU)	TTL Open Collector

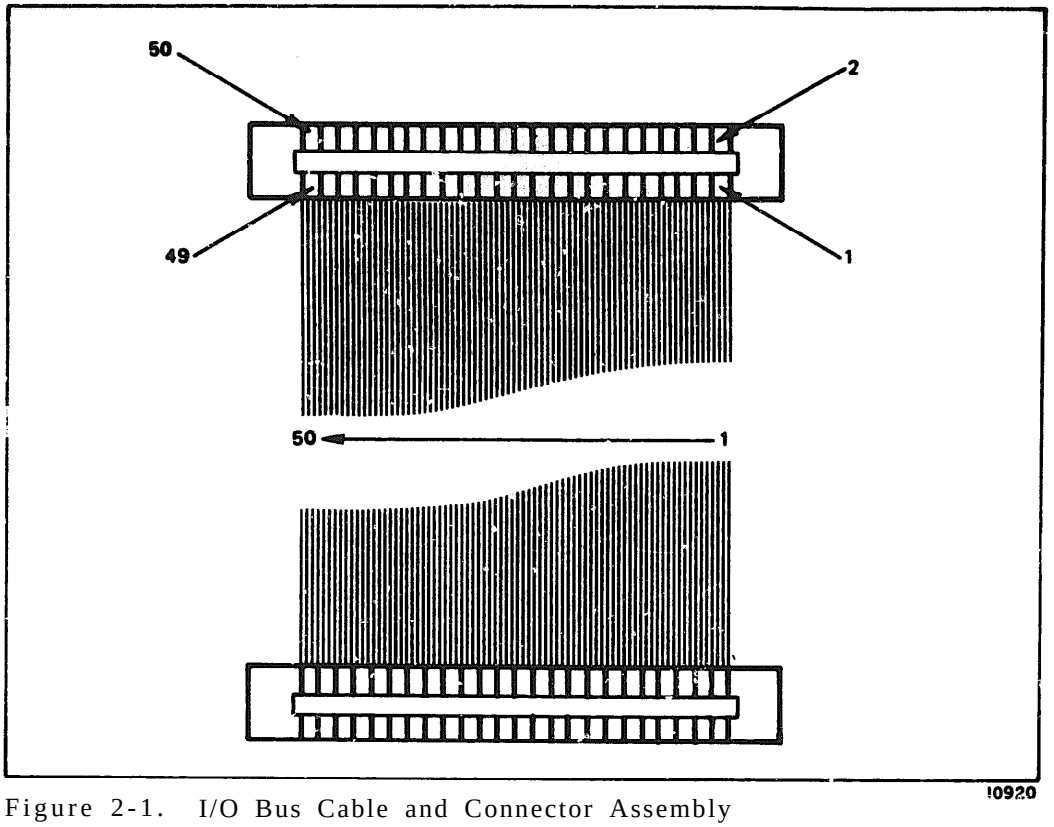


Figure 2-1. I/O Bus Cable and Connector Assembly

Physically the interface comprises the following cable assemblies:

- Cable assembly J1/P1.
- Cable assembly J2/P2.
- Cable assembly J3/P3.
- Cable assembly J4/P4.
- Cable assembly J12/P12.
- Text cable assembly, P/N 102156.

2.2.1 Cable J1/P1

The J1/P1 cable is a custom manufactured cable (Table 2-2). The J1/P1 cable has an edge connector for the control panel, one for the CPU and one for each of the peripheral controllers in the system. All connectors on the cable are designated P1 and plug onto corresponding J1 designated PC edge contact strips on the logic boards. In single or dual chassis systems, the cable terminates in the control panel and in the last controller of the system. In a multi-chassis system configuration, the cable terminates in the control panel and in the Utility Controller and Distributor (UCD) board, located in the second chassis. The J1/P1 cable, together with its matched counterpart, the J2/P2 cable, constitutes the internal I/O bus.

2.2.2 Cable J2/P2

The J2/P2 cable is, like the J1/P1 cable, custom configured to fit a specific system and therefore, may differ from one system to another

(Table 2-3). All connectors on the cable are designated P2 and plug onto corresponding J2 designated PC edge contact strips on the logic boards. The J1/P1 and J2/P2 cables are used in pairs, and for each system, are physically and functionally identical. Together, the two cables constitute the internal I/O bus.

Table 2-2. J1/P1 Signal Designations

Signal Line	Signal Mnemonic	Signal Line	Signal Mnemonic	Signal Line	Signal Mnemonic
J1-01	DIB06-	J1-18	EKO-	J1-35	GROUND
J1-02	DIB14-	J1-19	GROUND	J1-36	INT11-
J1-03	DIB04-	J1-20	STRB-	J1-37	GROUND
J1-04	DIB01-	J1-21	GROUND	J1-38	INT09-
J1-05	DIB00-	J1-22	DMAP1+	J1-39	GROUND
J1-06	DIB15-	J1-23	GROUND	J1-40	INT14-
J1-07	DIB12-	J1-24	INT15-	J1-41	GROUND
J1-08	DIB13-	J1-25	GROUND	J1-42	DMAP3+
J1-09	DIB10-	J1-26	DMAP2+	J1-43	GROUND
J1-10	DIB11-	J1-27	GROUND	J1-44	PCLK-
J1-11	DIB07-	J1-28	INT13-	J1-45	GROUND
J1-12	DIB02-	J1-29	GROUND	J1-46	DA05-
J1-13	DIB03-	J1-30	INT12-	J1-47	OF2-
J1-14	DIB05-	J1-31	GROUND	J1-48	OF0-
J1-15	DIB08-	J1-32	INT08-	J1-49	DA01-
J1-16	DIB09-	J1-33	GROUND	J1-50	OF1-
J1-17	GROUND	J1-34	INT10-		

Table 2-3. J2/P2 Signal Designations

Signal Line	Signal Mnemonic	Signal Line	Signal Mnemonic	Signal Line	Signal Mnemonic
J2-01	DMRQ-	J2-18	DOB02-	J2-35	GROUND
J2-02	GROUND	J2-19	DOB00-	J2-36	DMAMS-
J2-03	DMRS-	J2-20	DOB09-	J2-37	GROUND
J2-04	GROUND	J2-21	DOB03-	J2-38	DMAST-
J2-05	SYRST-	J2-22	DOB10-	J2-39	GROUND
J2-06	GROUND	J2-23	DOB14-	J2-40	ALOAD+
J2-07	DMALD-	J2-24	DOB08-	J2-41	PFFIP-
J2-08	GROUND	J2-25	DOB15-	J2-42	ALOAD-
J2-09	SPARE	J2-26	GROUND	J2-43	GROUND
J2-10	DOB11-	J2-27	BUSY+	J2-44	DA00-
J2-11	DOB13-	J2-28	GROUND	J2-45	DA02-
J2-12	DOB12-	J2-29	DMOS-	J2-46	DA03-
J2-13	DOB07-	J2-30	PRLD-	J2-47	DA04-
J2-14	DOB04-	J2-31	GROUND	J2-48	KF0-
J2-15	DOB05-	J2-32	DMACW1-	J2-49	KF1-
J2-16	DOB06-	J2-33	GROUND	J2-50	KF2-
J2-17	DOB01-	J2-34	DMACW0-		

2.2.3 Cable J3/P3

The J3/P3 cable comes in two versions, a standard cable and a custom designed cable (Tables 2-4a and 2-4b). With either version, the connectors on the cable are designated P3 and plug onto corresponding J3 designated PC edge contact strips on the logic boards. In all systems, regardless of configuration, the standard J3/P3 cable connects the CPU to the control panel (Table 2-4a). In expanded system configurations of more than two chassis, the custom J3/P3 cable connects the UCD in

Table 2-4a. J3/P3 Signal Designations, CPU to Control Panel

Signal Line	Signal Mnemonic	Signal Line	Signal Mnemonic	Signal Line	Signal Mnemonic
J3-01	SCTFP-	J3-18	BEQ-	J3-35	GROUND
J3-02	FPIR02	J3-19	GROUND	J3-36	MSW-
J3-03	GROUND	J3-20	FPIR01-	J3-37	GROUND
J3-04	BOVF	J3-21	GROUND	J3-38	MEDI-
J3-05	GROUND	J3-22	KSSW3+	J3-39	GROUND
J3-06	FPIR00	J3-23	GROUND	J3-40	GROUND
J3-07	GROUND	J3-24	KSSW1+	J3-41	GROUND
J3-08	FPIR03	J3-25	GROUND	J3-42	FPR+
J3-09	GROUND	J3-26	KSSW0+	J3-43	GROUND
J3-10	GROUND	J3-27	GROUND	J3-44	GROUND
J3-11	GROUND	J3-28	RUNLTE-	J3-45	GROUND
J3-12	BLT-	J3-29	GROUND	J3-46	PSW-
J3-13	GROUND	J3-30	RUNSW-	J3-47	GROUND
J3-14	BGT-	J3-31	GROUND	J3-48	INITP-
J3-15	GROUND	J3-32	STEPSW-	J3-49	GROUND
J3-16	KSSW2+	J3-33	GROUND	J3-50	RSMRL-
J3-17	GROUND	J3-34	WIRM-		

Table 2-4b. J3/P3 Signal Designations, UCD to ED

Signal Line	Signal Mnemonic	Signal Line	Signal Mnemonic	Signal Line	Signal Mnemonic
J3-01	DEK0-R	J3-18	DINT08-	J2-35	DDB08-R
J3-02	DEK0-	J3-19	DDB00-R	J3-36	DDB08-
J3-03	DINT15-R	J3-20	DDB00-	J3-37	DDB09-R
J3-04	DINT15-	J3-21	DDB01-R	J3-38	DDB09-
J3-05	DINT14-R	J3-22	DDB01-	J3-39	DDB10-R
J3-06	DINT14-	J3-23	DDB02-R	J3-40	DDB10-
J3-07	DINT13-R	J3-24	DDB02-	J3-41	DDB11-R
J3-08	DINT13-	J3-25	DDB03-R	J3-42	DDB11-
J3-09	DINT12-R	J3-26	DDB03-	J3-43	DDB12-R
J3-10	DINT12-	J3-27	DDB04-R	J3-44	DDB12-
J3-11	DINT11-R	J3-28	DDB04-	J3-45	DDB13-R
J3-12	DINT11-	J3-29	DDB05-R	J3-46	DDB13-
J3-13	DINT10-R	J3-30	DDB05-	J3-47	DDB14-R
J3-14	DINT10-	J3-31	DDB06-R	J3-48	DDB14-
J3-15	DINT09-R	J3-32	DDB06-	J3-29	DDB15-R
J3-16	DINT09-	J3-33	DDB07-R	J3-50	DDB15-
J3-17	DINT08-R	J3-34	DDB07-		

in the second chassis to the Expansion Distributor(s) in successive chassis (Table 2-4b). Together with its matched counterpart, cable J4/P4, the custom J3/P3 cable constitutes the external I/O bus in expanded system configurations.

2.2.4 Cable J4/P4

The J4/P4 cable is a custom designed cable (Table 2-5). All connectors on the cable are designated P4 and plug onto corresponding J4 designated PC edge contact strips on the logic boards. In all systems, regardless of configuration, one J4/P4 cable interconnects the CPU and all memory boards in the system. Additionally, in expanded system configurations of three or more chassis, a second J4/P4 cable is used to connect the UCD in the second chassis to the Expansion Distributor(s) in successive chassis. The J3/P3 and J4/P4 cables are used in matched pairs and for each particular system, are physically and functionally identical. Together they constitute the external I/O bus in expanded system configurations.

2.2.5 Cable J12/P12

The J12/P12 cable is a custom cable used only in system configurations that comprise more than two chassis (Table 2-6). The connectors on the cable are designated as P12 and plug onto the corresponding J12 designated PC edge contact strips of the UCD and Expansion Distributor boards, where the cable constitutes the DMA expansion bus.

2.2.6 Test Cable

The test cable enables temporary modification of the interface cabling to facilitate the checkout of a logic board, placed in the test position of the main chassis. (Figure 2-2).

Table 2-5. J4/P4 Signal Designations

Signal Line	Signal Mnemonic	Signal Line	Signal Mnemonic	Signal Line	Signal Mnemonic
J4-01	DPFFIP-R	J4-18	DKF1-	J4-35	DINT07-R
J4-02	DPFFIP-	J4-19	DKF2-R	J4-36	DINT07-
J4-03	DDAJO-R	J4-20	DKF2-	J4-37	DINT06-R
J4-04	DDA00-	J4-21	DOF0-R	J4-38	DINT06-
J4-05	DDA01-R	J4-22	DOF0-	J4-39	DINT05-R
J4-06	DDA01-	J4-23	DOF1-R	J4-40	DINT05-
J4-07	DDA02-R	J4-24	DOF1-	J4-41	DINT04-R
J4-08	DDA02-	J4-25	DOF2-R	J4-42	DINT04-
J4-09	DDA03-R	J4-26	DCF2-	J4-43	DINT03-R
J4-10	DDA03-	J4-27	DPCLK+R	J4-44	DINT03-
J4-11	DDA04-R	J4-28	DPCLK+	J4-45	DINT02-R
J4-12	DDA04-	J4-29	DSTRB+R	J4-46	DINT02-
J4-13	DDA05-R	J4-30	DSTRB+	J4-47	DINT01-R
J4-14	DDA05-	J4-31	DSYRST+R	J4-48	DINT01-
J4-15	DKF0-R	J4-32	DSYRST+	J4-49	DINT00-R
J4-16	DKF0-	J4-33	DPRLD+R	J4-50	DINT00-
J4-17	DKF1-R	J4-34	DPRLD+		

Table 2-6. J12/P12 Signal Designations

Signal Line	Signal Mnemonic	Signal Line	Signal Mnemonic	Signal Line	Signal Mnemonic
J12-01	DDMAP3+R	J12-11	DDMALD-	J12-21	DDMAST-
J12-02	DDMAP3+	J12-12	DDMALD-R	J12-22	DDMAST-R
J12-03	DDMAP2+R	J12-13	DDMRS-	J12-23	DDMAS-
J12-04	DDMAP2+	J12-14	DDMRS-R	J12-24	DDMAS-R
J12-05	DDMAP1+R	J12-15	DDMRQ-	J12-25	DDMACW1-
J12-06	DDMAP1+	J12-16	DDMRQ-R	J12-26	DDMACW1-R
J12-07	DDMOS-R	J12-17	DALOAD+	J12-27	DDMACW0-
J12-08	DDMOS-	J12-18	DALOAD+R	J12-28	DDMACW0-R
J12-09	DBUSY-R	J12-19	DALOAD-		
J12-10	DBUSY-	J12-20	DALOAD-R		

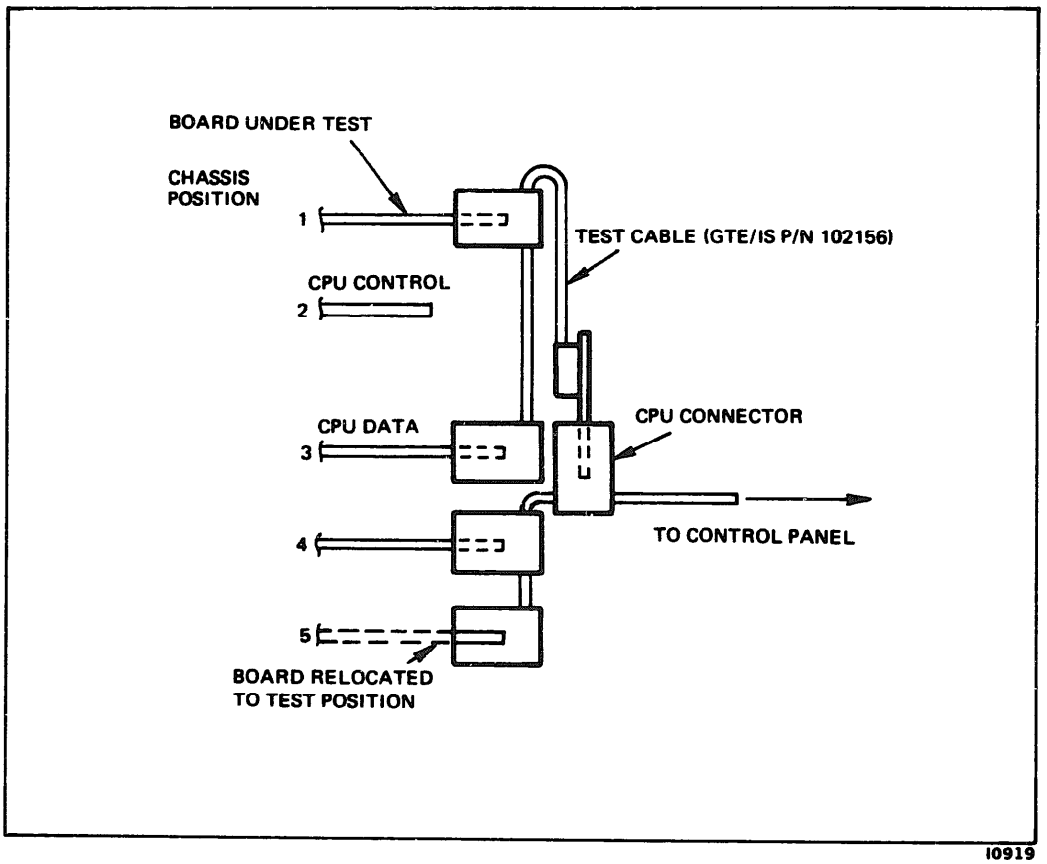


Figure 2-2. Interface Modification for Board Test

2.3 FUNCTIONAL DESCRIPTION

All communications and data transfers within the IS/1000 Processor system take place over the interface structure. All interface lines are connected to all controllers in parallel; however, only one controller at a time may use the lines. The CPU can drive 14 inches of I/O bus and up to eight peripheral device controllers or seven controllers and a Utility Controller and Distributor (UCD). If more than eight controllers are required by the system, or if the controllers are located more than 14 inches away from the CPU, a UCD must be used to buffer the I/O bus and to transfer I/O information to or from an Expansion Distributor (ED). A UCD can handle up to eight EDs or 25 feet of I/O bus. Each ED in turn can drive up to eight peripheral device controllers.

Functionally the interface comprises the following channels:

- CPU to Control Panel. This channel is constituted by the J3/P3 cable and portions of the J1/P1 and J2/P2 cables. (Figure 2-3). See Tables 2-2 and 2-3 for signal line designations.
- CPU to memory. This channel is constituted by the J4/P4 cable. (Figure 2-4). See Table 2-5 for signal line designations.

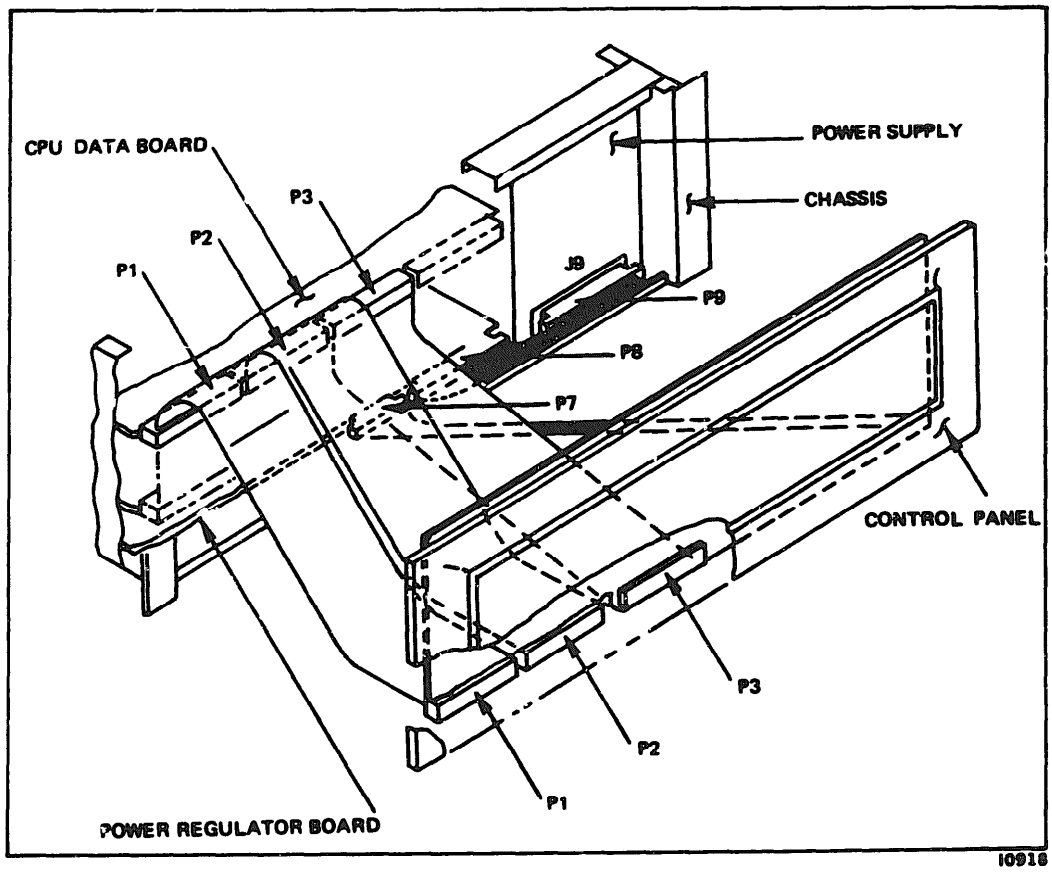


Figure 2-3. Control Panel Cabling

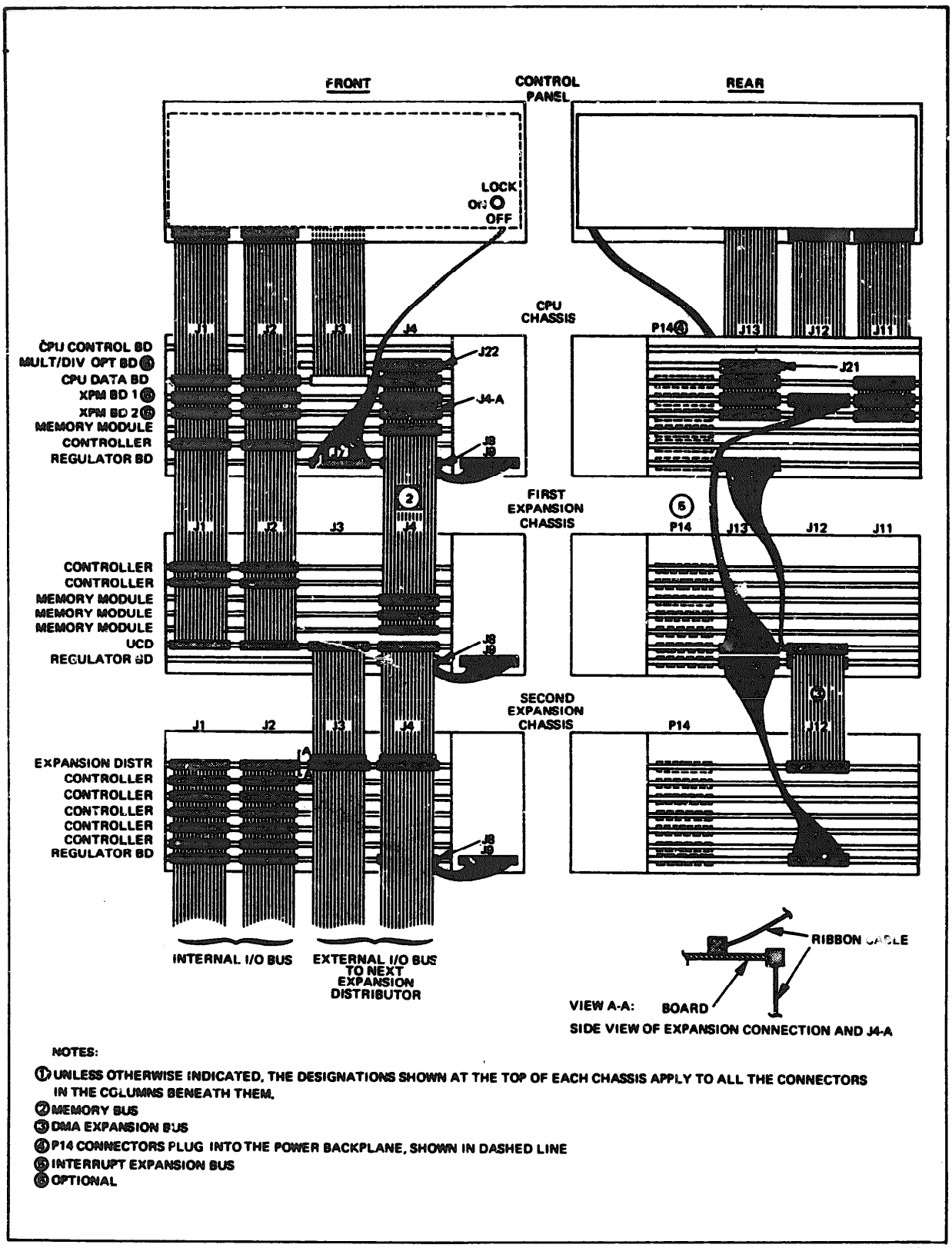


Figure 2-4. Internal and External Cable Configuration

- CPU to peripheral device controllers. These channels are constituted by the J1/P1 and J2/P2 cables in system configurations with standard interface; additionally, by cables J3/P3 and J4/P4 in system configurations with expansion interfaces (Figure 2-4). See Tables 2-2 thru 2-6 for signal line designations.

- Memory to peripheral device controllers, i-e., DMA. This channel is established by cables J1/P1, J2/P2, J3/P3 and J4/P4 in system configurations with standard interface; additionally, by cable J12/P12 in system configurations with expansion interfaces (Figure 2-4). See Tables 2-2 thru 2-6 for signal line designations.

In systems comprised of three or more chassis, the interface is extended with an expansion or external I/O bus. In this case the use of a UCD working in 'conjunction with from one to eight EDs, is required.

Regardless of system configuration, the heart of the interface communication concept is the priority interrupt scheme and its effective use during I\O operations.

For I/O operations with peripheral devices capable of data transfer rates of one million words per second and more, the DMA channel is available. The direct memory access is accomplished over the existing interface cable system, through a functional channel created by special logic.

2.3.1 Internal I/O Bus

All peripheral device controllers are connected to the internal I/O bus. The output lines of the internal I/O bus are originated, and the input lines terminated, by the I/O section in the CPU or in the ED.

The internal I/O lines, originating or terminating in the CPU assembly, are shown in Figure 2-5, and fall in three categories:

- Control signals.
- Interrupt signals.
- Data.

2.3.1.1 Control Signals

Control signals provide information to the controllers as to the type of function to be performed. Part of the instruction specifies the controller being addressed by the I/O instruction. The other parts of the instruction, are the K and O fields. The K-field defines the class of the instruction, the O-field defines the specific function to be performed for the particular instruction class specified by the K-field.

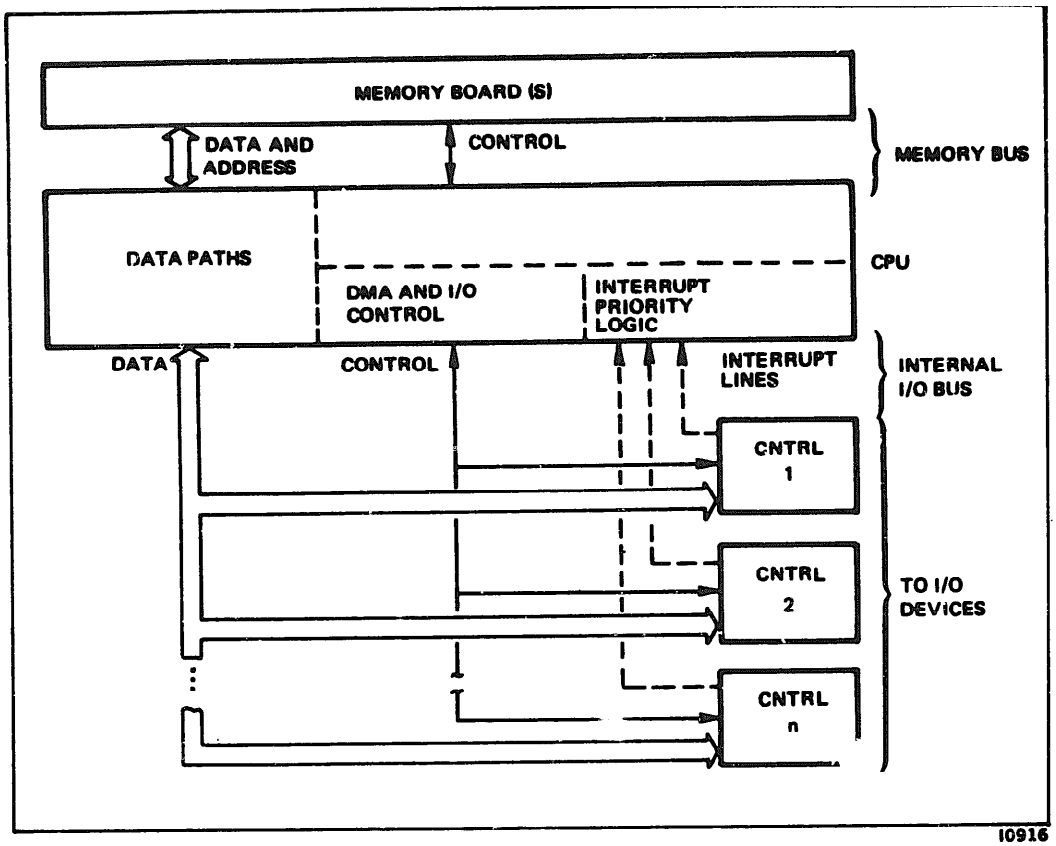


Figure 2-5. Interface, Internal I/O Bus

A strobe signal is used to enable the controller to accept the decoded command information, to transfer data in or out, or to initiate execution of a function.

The CPU provides a free-running 4-MHz clock for use by some controllers. The clock is not synchronous with the regular CPU clock but rather with the strobe signal.

A system reset is generated during power-up and power-down sequences, and when the RESET switch on the control panel is pressed while the CPU is in the Halt mode. The latter Reset condition causes all controllers to finalize current activity and become ready to accept new Commands, all peripheral devices to be halted and all status flags to be reset (except those requiring operator intervention).

Autoload signals are provided for use when the autoload function is to be activated by peripheral devices using the I/O bus. The autoload condition causes execution of a special sequence that transfers a program from a ROM in the CPU to the memory and starts execution of that program. An autoload can be initiated in three ways:

- Control panel initiated autoload.
- Power panel initiated autoload.
- Blank panel initiated autoload.

2.3.1.2 Interrupt Lines

The I/O bus contains special lines for the eight regular external interrupts. Through use of an optional Expanded Performance Module (XPM) the number of lines can be functionally increased to 16. This is accomplished strictly through enhancement logic; physically, the number of lines on the internal I/O bus remains eight.

2.3.1.3 Data Lines

Output data is transferred from the CPU to the controllers via the Data Out bus lines. Input data is transferred from the controllers to the CPU via the Data In bus lines.

2.3.2 External I/O Bus

The external I/O bus is used to extend the physical length of the I/O bus and to provide the ability to attach up to eight EDs. The external I/O bus is not intended for peripheral device controller interfaces because of the critical drive and termination require-- ments. The external I/O bus originates in the UCD.

Line drivers and receivers are provided in the UCD and the EDs to maintain the logic levels and permit a fanout of eight loads on each line.

The external I/O bus may extend up to 25 feet in length. Since up to six controller boards can be installed in an expansion chassis that is 7 inches high, the standard I/O bus length is ample (Figures 2-5 and 2-6). Logic implementation of the I/O bus expansion feature is shown in Figure 2-7.

2.3.3 Priority Interrupt System

An interrupt is generated when a peripheral device or a system function requires attention by the CPU. Interrupt sources are given interrupt priorities on the basis of importance and data transfer rate. Interrupt sources can both be external and internal to the CPU assembly. Internal interrupts are associated with automatic functions such as power failure detection and error conditions. External interrupts are associated with peripheral device servicing.

The priority interrupt system has control logic for:

- Active interrupt storage.
- Interrupt enable/disable.
- Interrupt recognition.
- Priority recognition.
- Priority selection.
- Generation of interrupt trap addresses.

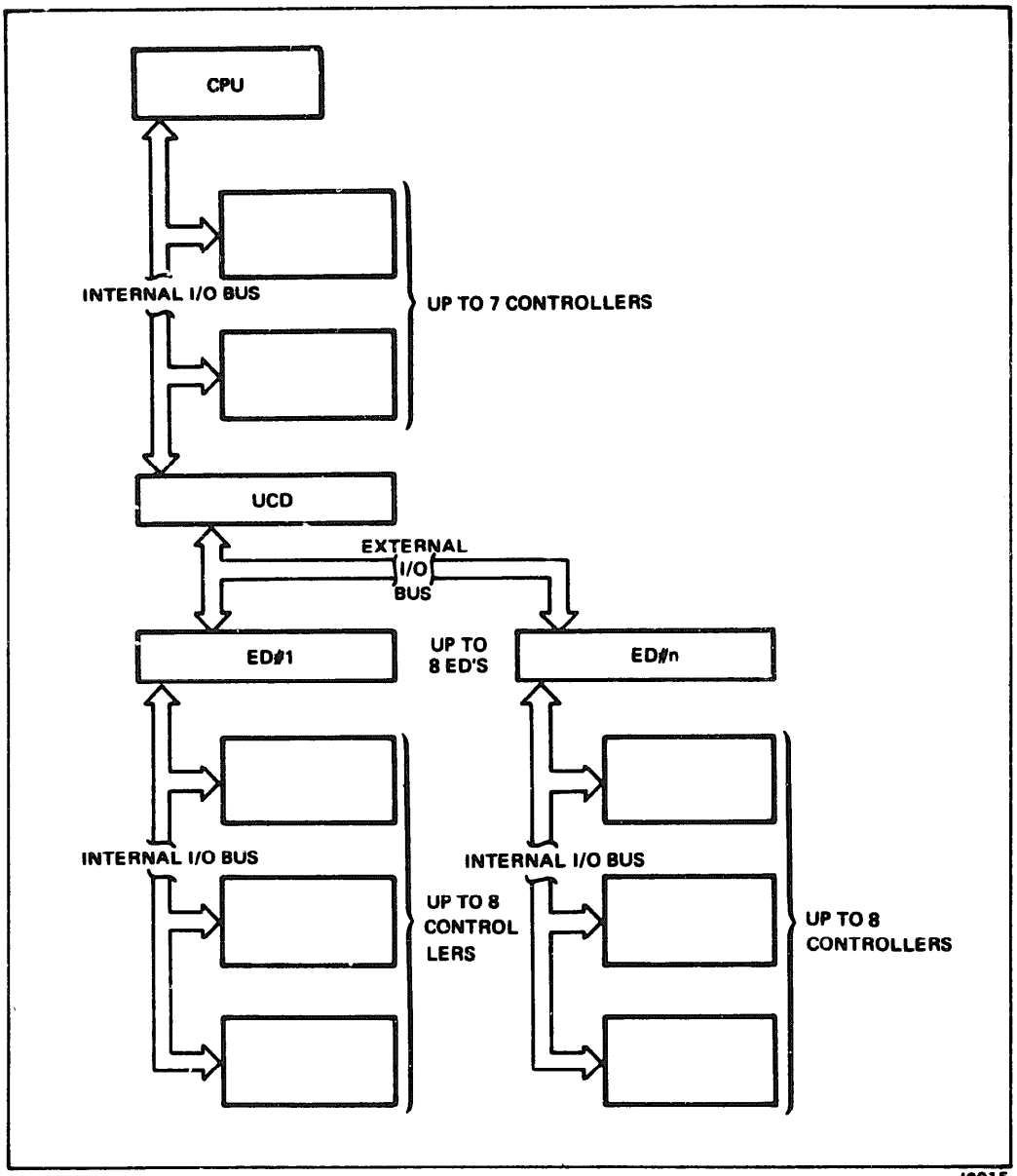


Figure 2-6. Expanded Interface

The internal interrupts which are associated with the CPU have the following priorities, (0 is highest).

0. Power fail/restart.
1. Instruction trap.
2. Memory protect*.
3. Privileged instruction interrupt*.

*XPM option

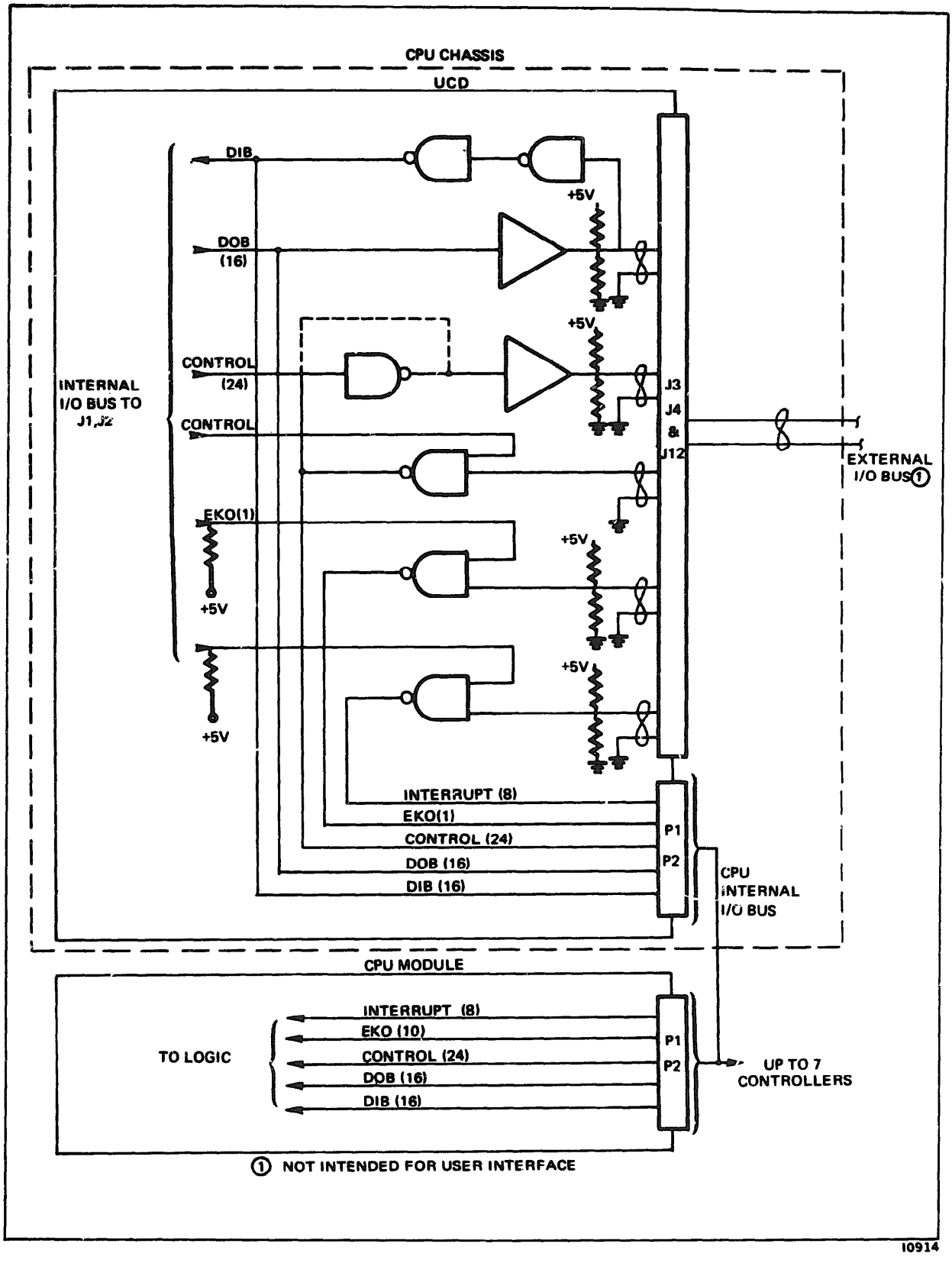


Figure 2-7. Expansion Interface Logic (Sheet 1 of 2)

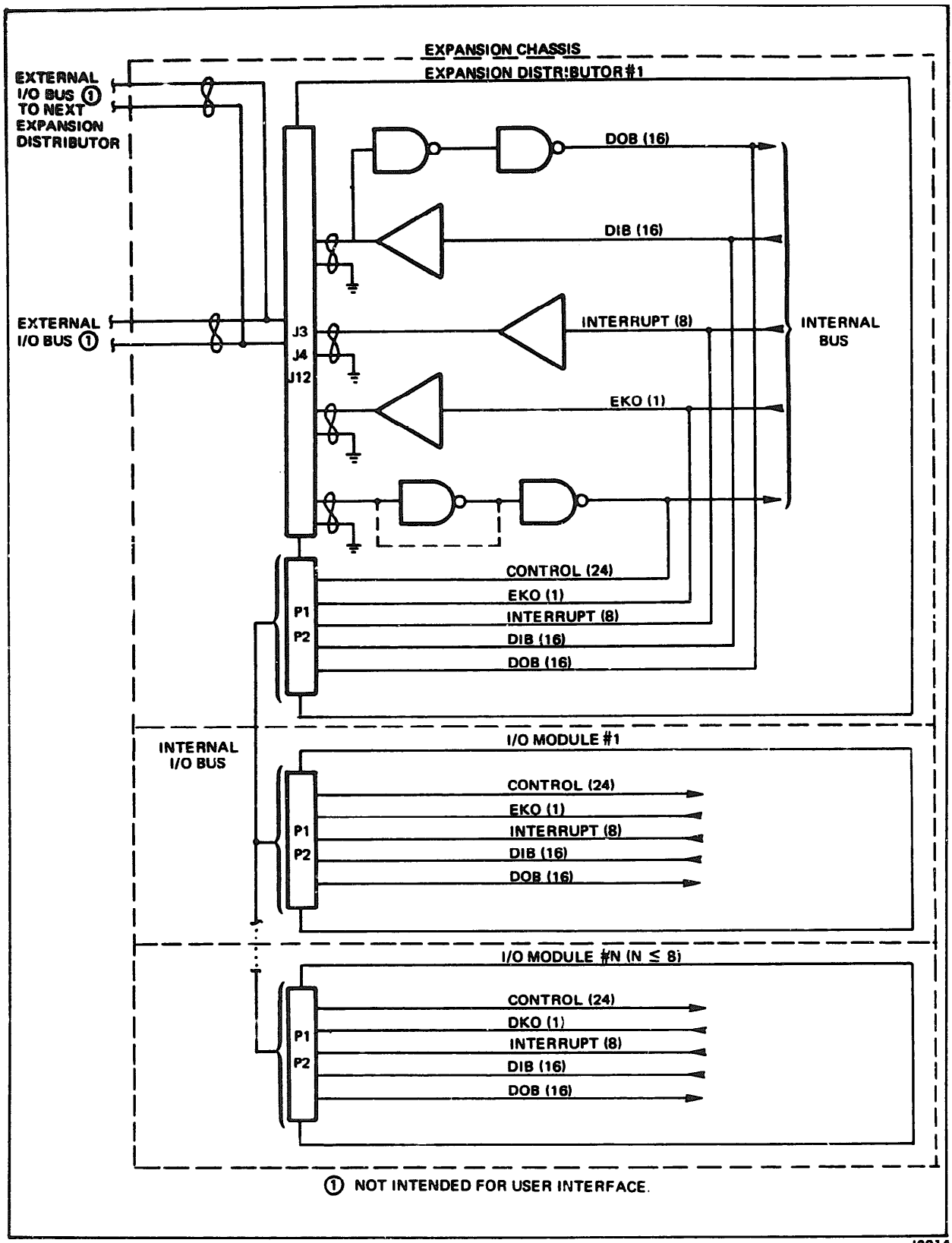


Figure 2-7. Expansion Interface Logic (Sheet 2 of 2)

The external interrupts have the following priorities (0 is highest).

0. General purpose*.
1. General purpose*.
2. General purpose*.
3. General purpose*.
4. General purpose*.
5. General purpose*.
6. General purpose*.
7. General purpose*.
8. General purpose.
9. General purpose.
10. General purpose.
11. General purpose.
12. General purpose.
13. General purpose.
14. Teleprinter.
15. General purpose.

NOTE: The controller can be patched to only eight-interrupts through patches on the controller board. The expansion to sixteen interrupts is provided through patches on the ED.

Internal interrupts have priority over external interrupts.

When two or more interrupts of any kind are active, priority logic in the CPU selects the appropriate interrupt for servicing. The logic also enables higher-priority interrupts to interrupt lower-priority interrupts in the process of being serviced, without loss of the lower priority status. Peripheral device controllers contain plugboards to establish the address and interrupt(s) of that device, with each interrupt patched for a specific priority level. The plugboards enable the ready reassignment of priority level or changing of the address at any time without etch pattern modifications. It is not necessary that the interrupt number coincides with the device number, but generally these numbers do correspond.

When two or more peripheral devices share a single interrupt line, they can be considered as having a level of priority within a level. Their priority is determined first by the relative position of the shaded interrupt line in the priority interrupt system, and second, by the priority established by the subroutine that services the

*XPM option

shared interrupt. For those controllers that can share an interrupt, a plugboard is provided in the controller to select which data line is to respond to the ICI (interrogate common interrupt) I/O instruction.

As many as 16 peripheral devices can share any one of four common interrupt lines. Any combination of four interrupt lines may be used as common interrupts. The two most-significant bits of the peripheral device address are decoded for the ICI instruction. Thus, four distinct codes are available for selecting one of four interrupt lines.

2.3.4 Direct Memory Access

Through the DMA channel, direct data transfers between the memory and the I/O bus are made possible. Each data transfer requires one memory cycle of 750 ns for a maximum transfer rate of 1.33 MHz. However, due to inherent delays, the practical data transfer rate is 1.1 MHz*. When the data transfer rate falls below 1.1 MHz*, the DMA channel could free the CPU to enable processing of program instructions. To use the DMA channel, the processor must condition the peripheral device via the I/O bus. Then, when the peripheral device requires service, it requests access to the memory via a DMA request line.

At the beginning of every memory cycle, the processor synchronizes and recognizes any requests for direct memory access that are being made. This assures a no longer than 750-ns wait for a DMA cycle and as long as the DMA request line remains active, every memory cycle is available. However, delays longer than 750 ns are possible, when:

- Another peripheral device is using the DMA channel.
- The CPU has a power failure.
- An I/O instruction is being executed, since the same I/O bus is used for both, ordinary input/output and DMA operations.

*1.09 MHZ when XPM option used

SECTION 3
PRINCIPLES OF OPERATION

3.1 AUTOLOAD OPERATION

Autoload signals, ALOAD+ and ALOAD- are provided for use when the autoload function is to be activated by devices on the I/O bus. Autoload causes execution of a special sequence that transfers a program from a ROM in the CPU to the memory and starts execution of that program. An autoload operation may be initiated in three ways:

- Control Panel Autoload.
- Power Panel Autoload.
- Blank Panel Autoload.

3.1.1 Control Panel Initiated Autoload

With the control panel connected and the CPU in the Halt mode, the autoload function can be activated in one of two ways. If the key on the front panel is in the ON position, the load button on the control panel activates the autoload function when it is pressed and released. If the key on the front panel is in the LOCK position, the autoload function is activated via the I/O bus if term ALOAD+ goes high and term ALOAD- goes low simultaneously, for approximately 10 us. If the autoload operation is to be initiated via the I/O has and from the control panel as well, and it is desired to operate autoload from the front panel, the LOAD switch on the control panel must have additional controls, corresponding to the key on the control panel that disables the I/O bus switch controls of ALOAD+ and ALOAD-. Therefore, if the autoload operation is enabled simultaneously by key functions from the control panel and the I/O bus, it can not be activated by both, but only by one of the key functions.

3.1.2 Power Panel Initiated Autoload

The power panel autoload has the same functions and interlocks as the control panel, but in addition it brings up term SYRST- (system reset) which resets the CPU and all peripheral device controllers when the autoload function is activated, i.e., terms ALOAD+ and ALOAD- go true. This reset operation is a necessity since the power panel has only one switch, i.e., LOAD '(autoload). This switch must reset the CPU and all controllers. The following functions occur when the LOAD switch is activated, with the power panel connectad to the CPU:

- Activate Autoload.
- Reset I/O
- Reset CPU.

The activation of the autoload function from the power panel or via the I/O bus is not synchronized with the CPU timing. Therefore, if the CPU is executing programs when autoload is activated, the

resetting of the CPU will probably alter register contents in the CPU. The memory interface is so designed that resetting the CPU should not affect the reading of data from memory but if the CPU is in the middle of a write into memory operation when it is reset, the data that is written into the memory can not be assumed to be correct.

3.1.3 Blank Panel Initiated Autoload

Since the CPU does not require the control panel nor the power panel to operate, a blank panel may be used with it. The autoload is then controlled exclusively from the I/O bus. This eliminates the interlocking concept but still enables the CPU and I/O controllers to be reset. The activation of an autoload operation via the I/O bus is not synohronized with the CPU timing, therefore, resetting of the CPU will probably alter the contents of some registers in the CPU. The memory interface is be signed so that resetting of the CPU will not affect data already stored in memory but data that is being stored may be altered.

3.2 CONTROL OPERATIONS

The CPU communicates with all peripheral devices and their associated controllers, via the I/O bus structure (Figure 3-1). When the CPU is ready to communicate with a controller, the CPU places the desired controller address and command signals plus data (if applicable) on the I/O bus. Only the addressed controller recognizes the address and responds to the instruction.

The device address of the controller comes from bits 10 thru 15 of the I Register. The device address is sent to indicate the particular device controller being addressed by the I/O instruction. All controllers decode the device address, but only the addressed controller can respond. If an I/O controller is addressed but does not respond by sending an echo signal, the CPU does a Branch-and-Store-P (BSP) instruction to the address specified by the second word of the I/O instruction. The I/O bus mnemonics for the device address bits are DA00 thru DA05, corresponding to I-Register bits 10 thru 15, respectively.

Along with the device address, the K field and O field are transmitted to the controller. The K field, comprised of I-Register bits 4, 5 and 6, defines the class of instruction to be performed by the addressed controller. The I/O bus mnemonics for the K field are KF0- thru KF2-, corresponding to I-Register bits 4 thru 6, respectively.

The O field comprised of I-Register bits 7, 8 and 9, defines the specific function to be performed for a particular instruction class. The I/O bus mnemonics for the O field are OFO- thru OF2-, corresponding to I-Register bits 7 thru 9, respectively.

When all control lines have stablized, strobe term STRB- is generated to inform the controller to use the decoded command information to transfer data in or out, or to initiate execution of A function. The

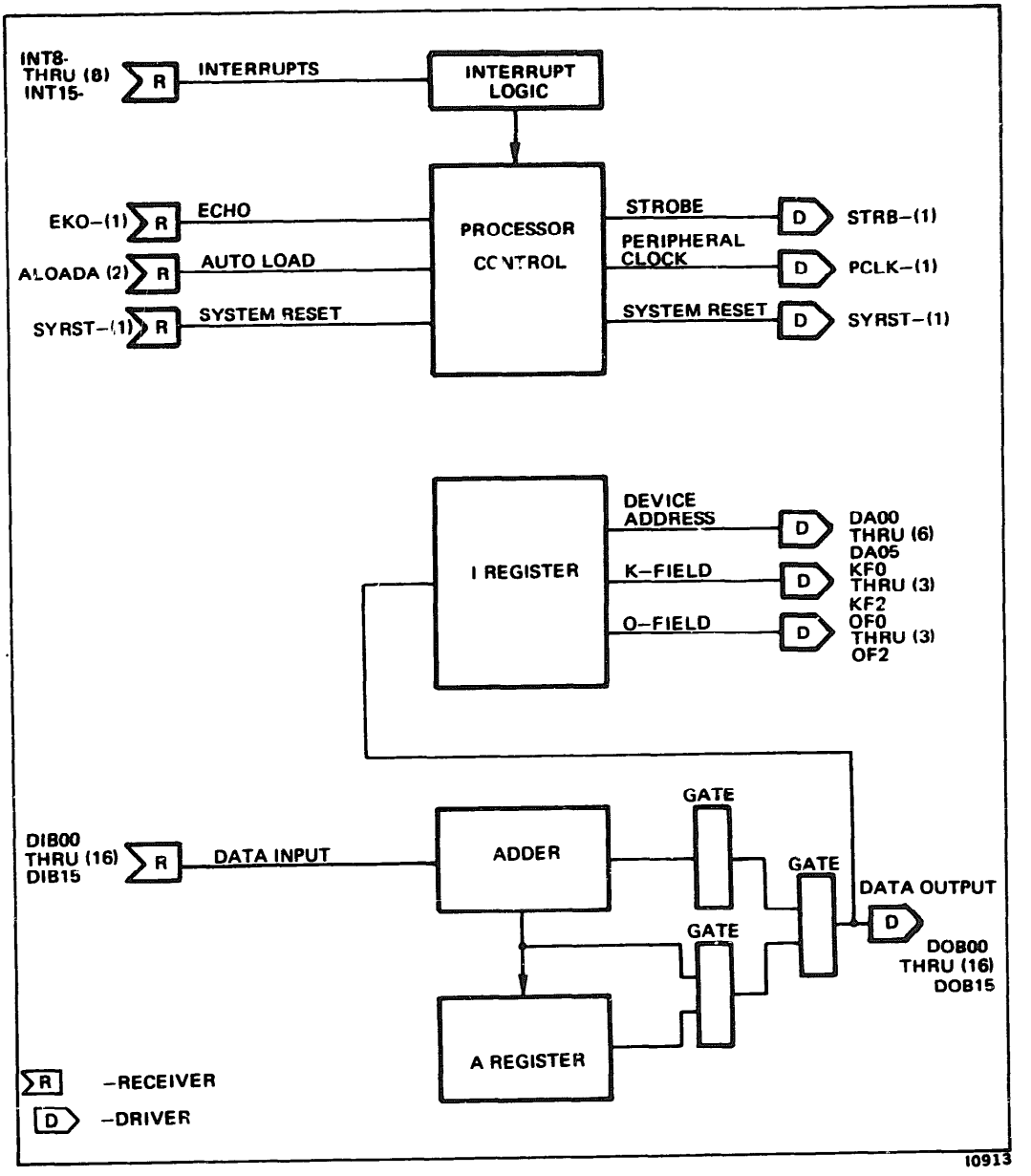


Figure 3-1. CPU Module Functional Interface

CPU stops processing and waits (as long as 1.3 us) for a response from the device controller. If a response is received in the form of term EKO-, the CPU resumes processing and turns off the STRB- and control signal. If a response is not received within 1.3 us, the CPU can opt to assume that no response is forthcoming. If a response is not received after 2 us, the CPU will assume a nonresponse condition and performs BSP to the address specified by the second word of the I/O instruction.

The CPU also generates a 4-MHz clock signal term PCLK, for use by certain controllers. Term PCLK is synchronous with term STRB.

When the RESET switch on the control panel is pressed with the CPU in the Halt mode, system reset term SRST- is generated. Term SRST-, which is also generated during power-up and power-down sequences, resets all status flags, stops all peripheral devices and clears all controllers, leaving them ready to accept new instructions.

3.3 INPUT/OUTPUT OPERATIONS

3.3.1 I/O Timing

The I/O bus is asynchronous in operation. A start signal, term STRB, is generated and the master clock is stopped in the CPU. When the controller responds with EKO, the master clock is restarted. This start/stop I/O timing method enables the I/O bus to be extended without communication failure, by producing variable signal delays. The extension of time however, adds directly to interrupt service time and thus decreases the number of CPU cycles or instructions that can be performed per unit of time, which may be critical.

Basic I/O timing originates in the CPU where a 4-MHz peripheral clock signal (PCLK) is derived from an 4-MHz crystal driven oscillator. The 4-MHz and 8-MHz signals are logically combined to set a strobe flip-flop during I/O machine sequence. Generation of the resulting STRB signal initiates the controller I/O sequence, as shown in Figure 3-2.

There are two I/O data transfer sequences:

- Input data transfer.
- Output data transfer.

3.3.2 Input Data Transfer

The input data transfer sequence is used for Word Transfer IA (WTI), Request Device Status (RDS) and Interrogate Common Interrupts (ICI) instructions. A timing diagram showing the relationship of the signals at the controller end, is shown in Figure 3-2. The input transfer is sequenced as follows:

- Control information in the from of the device address, K field and O field, is placed on the control lines at least 330 ns before STRB- is generated. The control information has therefore settled on the I/O bus and is stable when term STRB- is generated.
- Term STRB- is generated.
- Input data or status is placed on the DIB lines as soon as possible after STRB- has been received by the controller. Any delay in providing data adds directly to the I/O transfer time.
- Term EKO- is generated within 1.3 us after the activation of STRB. Term EKO- must occur on time or a simulated BSP instruction is executed. Data to be transferred is generated at least 50 ns before term EKO is brought up, to

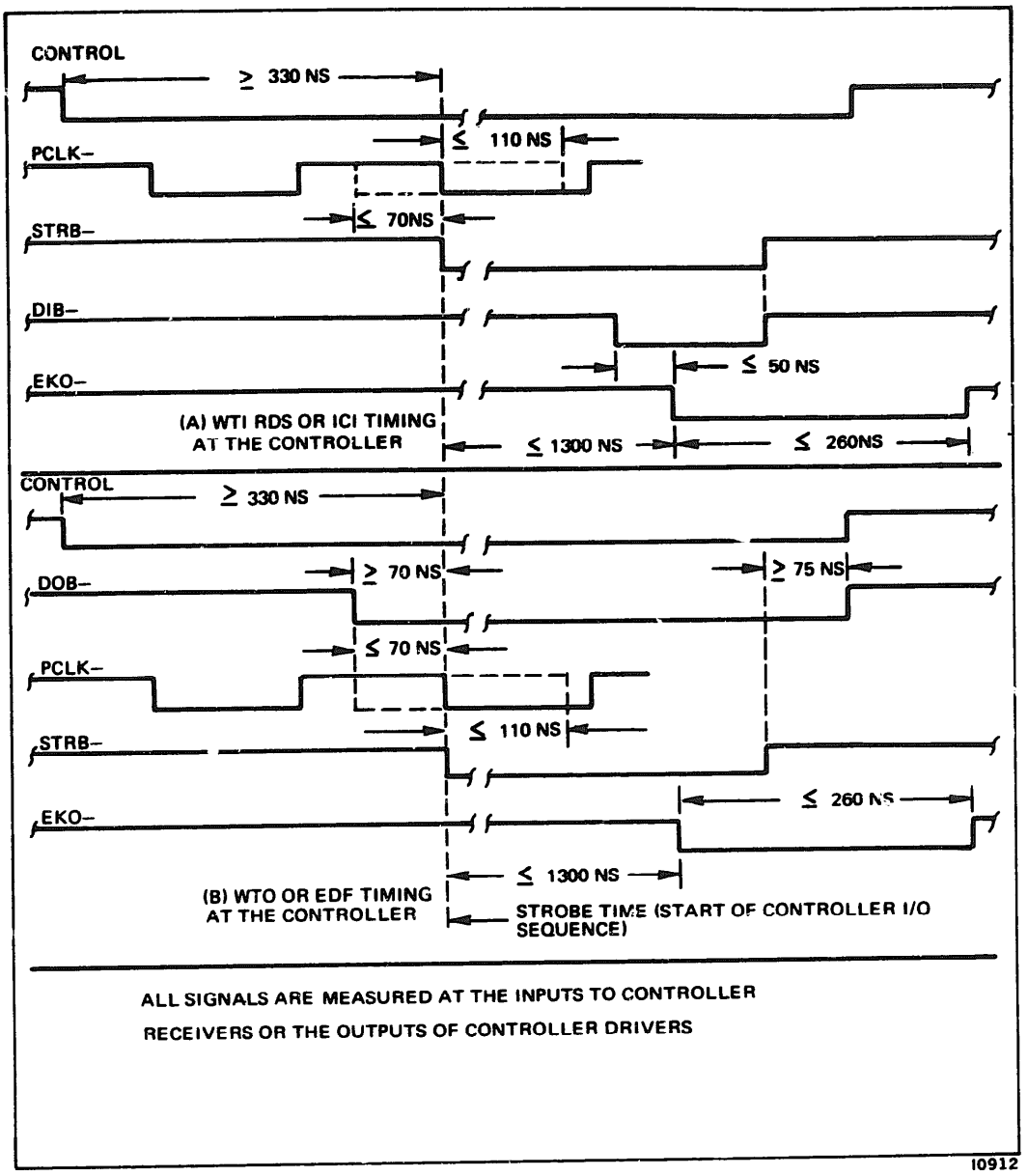


Figure 3-2. I/O Sequence Timing at Controller

ensure reliable gating at the CPU. If the instruction being executed is a WTI in response to an interrupt, the controller interrupt line must be reset within 50 ns after the leading edge of EKO.

- Term STRB- goes false. This discontinues the gating of data out of the controller.
- Control information ends.

3.3.3 Output Data Transfer

The output data transfer sequence is used for word transfer out (WTO) and execute device function (EDF) instructions. A timing diagram

showing the relationship of the signals at the controller end, is shown in Figure 3-2. The output transfer is sequenced as follows:

- Control information in the form of the device address, K field and O field is placed on the control lines at least 330 ns before term STRB- is generated. All decoding of control signals must be accomplished within this period.
- Output data or device function information is placed on the DOB lines at least 70 ns before term STRB is generated to ensure reliable gating at the controller.
- Term STRB- is generated.
- Term EKO- is generated within 1.3 us after the activation of STRB-. Term EKO- must occur on time or a simulated BSP instruction is executed. If the instruction being executed is a WTO in response to an interrupt, terms EKO and WTO will reset the controller interrupt line. The line must be reset within 50 ns of the leading edge of term EKO.
- Term STRB- ends.
- Control information and data must remain active for at least 75 ns after the fall of STRB; this ensures reliable gating of data into the controller.

3.4 INTERRUPT OPERATIONS

Program interrupts provide the capability of responding to a condition that needs immediate service without requiring the program to check the status of a peripheral device. When a controller is ready to either provide or accept data, it interrupts the main program. This causes the program to branch to the appropriate interrupt service subroutine.

A fixed memory location (Table 3-1) is assigned to each program interrupt. Each such fixed interrupt memory location contains the address of the first location of the interrupt service subroutine associated with the corresponding program interrupt.

The CPU normally accepts the interrupt at the completion of the current instruction execution, except when a BSP, a Load Interrupt Enable (LIE), a Store Interrupt Enable (SIE), or an I/O instruction is being executed at the time the interrupt is set. In any of these cases, one additional instruction is executed before the interrupt is recognized. The BSP may either be programmed or simulated via a response to an interrupt or an I/O reject. When the interrupt is recognized by the CPU, an interrupt flip-flop (of which there is one for each interrupt line) is set to prevent further interrupts on that line or lower priority lines, until the interrupt has been processed. A simulated BSP is executed to the memory location specified in the fixed interrupt memory location.

The P-Register value of the interrupted program is stored in the first location of the interrupt service routine. It points to the

Table 3-1. Interrupt Memory and Device Address and Priority Assignment

Interrupt	Memory Address (Hexadecimal)	Interrupt (Hexadecimal)	Priority Class
Internal			
Power Fail/Restart	$0A	0	1
Instruction Trap	$0C	2	2
Memory Protect*	$0D	3	3
Privileged Instruction Interrupt*	$0E	4	4
External			
I/O Interrupt*	$10	0	5
I/O Interrupt*	$11	1	6
I/O Interrupt*	$12	2	7
I/O Interrupt*	$13	3	8
I/O Interrupt*	$14	4	9
I/O Interrupt*	$15	5	10
I/O Interrupt*	$16	6	11
I/O Interrupt*	$17	7	12
I/O Interrupt	$18	8	13
I/O Interrupt	$19	9	14
I/O Interrupt	$1A	A	15
I/O Interrupt	$1B	B	16
I/O Interrupt	$1C	C	17
I/O Interrupt	$1D	D	18
I/O Interrupt	$1E	E	19
I/O Interrupt	$1F	F	20

*XPM option

next instruction to be executed in the interrupted program. For the instruction trap interrupts, the P-Register value stored points to the next word in memory.

Interrupt service routine execution is completed and terminated by either a Branch and Reset Internal Interrupt (BRI) or a Branch and Reset External Interrupt (BRE) instruction, depending on whether the interrupt was internal or external, respectively.

All program interrupts are organized on a priority basis. There is a priority established among the two classes of interrupts (internal and external) as well as among the set of interrupts within each class. The interrupts are listed in Table 3-1 according to their assigned priority, with Power Fail/Restart having the highest priority. The priority determining logic in the processor selects the appropriate interrupt when two or more interrupts are pending. This logic also permits higher priority interrupts to interrupt lower priority interrupts, without loss of the lower priority status.

When the processor is in the Halt state, no program interrupts are recognized; when the processor is in the Wait state, all interrupts are recognized.

3.4.1 Internal Interrupts

The internal interrupts have the highest assigned priority. The internal interrupts are:

- Power-fail/restart.
- Instruction trap.
- Memory protect*.
- Privileged instruction interrupt*.

3.4.1.1 Power-Fail/Restart Interrupt

This function continuously monitors the ac input power. If the input voltage falls below 102 Vac and the CPU is in Run mode, a power-fail interrupt is initiated. The P--Register value is stored in memory by a simulated BSP instruction; however, since the same location is used for the restart interrupt, the P-Register value must be stored in another location by means of the P/R routine. The power-fail subroutine can be modified by the user but normally it stores the contents of all registers and all volatile flags, in memory. The subroutine must conclude with a Halt instruction.

The memory is disabled after approximately 1 ms, to protect the stored contents. On return of ac power to 105 Vac, the memory is enabled and the restart interrupt is generated. The restart subroutine can also be modified by the user but normally restores all registers and volatile flags and returns control to the interrupted program or to some other, specified program. A BRI instruction (for interrupt line number 0) must not be given prior to the halt during the power failure subroutine, but is required when terminating the restart subroutine.

The power-fail/restart subroutine can determine whether the interrupt was caused through a power-fail condition or through a restart operation, by examining the CPU status with a Request Internal Status (RIS) instruction. Bit position 0 of the CPU status (Figure 3-3) is set to ZERO whenever a restart takes place. After completion of the power-up routine, the BRI will set bit position 0 of the CPU status to ONE to provide the means for indicating the nature of a future power down, i.e., whether it is a restart operation or a power fail condition. RIS transfers CPU status to the A Register (volatile flags) for storage in memory in the event of a power failure. When power returns, Internal Control Function (ICF) is used to re-establish the status of the CPU status flags.

3.4.1.2 Instruction Trap Interrupt

This function enables non-implemented instructions to be detected. The use of such a non-implement&\ instruction results in an interrupt to a subroutine that interprets and executes the attempted instruction by means of a program subroutine.

*XPM option

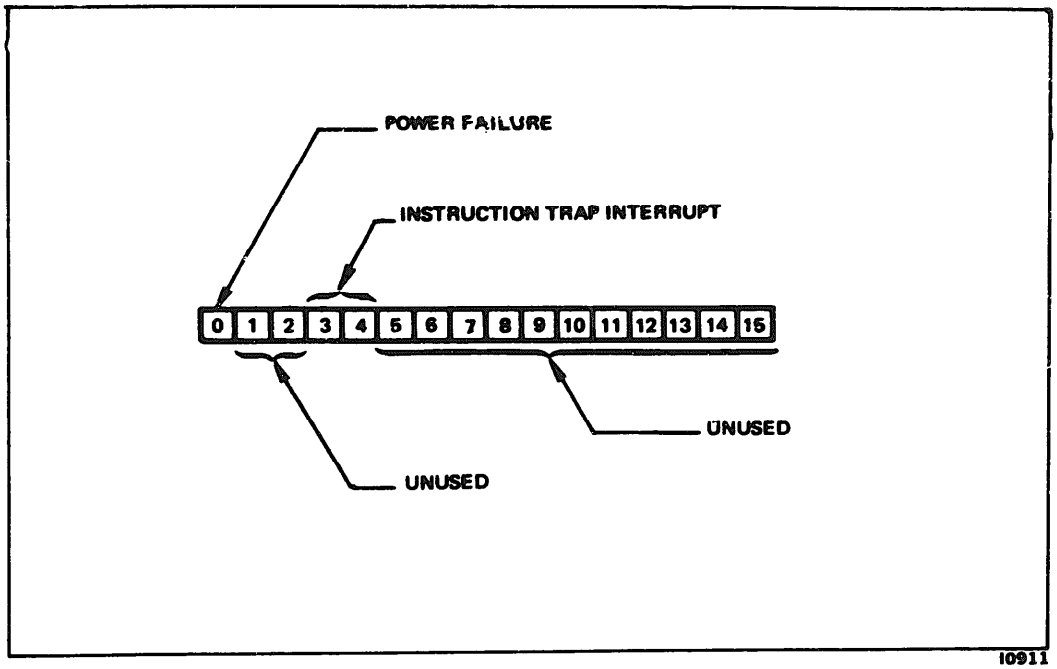


Figure 3-3. CPU Module Status Word

The instruction trap is also activated if a two-word memory reference (AAM, AMA, AMX, ANA, ANB, ANX, BSP, CAM, CBM, CXM, DIV, EOA, EOB, EOX, INC, LDA, LDB, LDX, ORA, ORX, SMA, SMB, SMX, STA, STB, STX) instruction utilizes addressing mode T-8, 9 or 12. The instructions that result in an instruction trap interrupt, includes

- Multiply/divide option (MUL, DIV).
- All instructions with a C field greater than or equal to 5 that use addressing mode T-8, 9 or 12.
- Non-implemented C-field 2 instructions.

The instruction trap interrupt results in the execution of a simulated BSP to the instruction trap subroutine via the interrupt memory location listed in Table 3-1. The instruction in the I Register is set to a BSP and executed, disturbing none of the registers or flags of the CPU.

The P Register value that is stored in memory points to the next instruction, if the instruction was a one-word instruction, or to the second word of the instruction, if the instruction was the first word of a two-word instruction. Decrementing this P Register value allows access to the instruction to be interpreted. If it is a two-word instruction, the P Register value stored must be incremented before returning to the main program. The instruction trap subroutine is terminated with BRI (for interrupt line number 2).

3.4.1.3 Memory Protect Interrupt

The memory protect feature is a XPM option available when the XPP is used with a model 4500-02 CPU. This option provides program storage protection by generating a memory protect interrupt whenever a program, during execution, violates the memory segment boundaries of other independent programs. The memory protect feature is implemented as follows.

A memory protect mask is stored for each segment. The states of the no-page flag and write-protect flag for each segment are established.

The real address is checked against the applicable memory protect mask during address construction. If the real address references a memory location outside the physical limits defined by the memory protect mask, the maximum-page error indicator is set. The state of the maximum-page error indicator is detected by the Privileged and Memory Protect interrupt Generator which then sends a memory Protect interrupt to the CPU.

When a segment is addressed for which the no-page flag is set (indicating the segment does not exist), an error signal is generated. The error signal sets the no-page error indicator which results in a memory protect interrupt to the CPU.

An attempt to write into a write-protected segment (write-protect flag set) while the CPU is in the nonprivileged mode, results in the write-protect error indicator being set. The set state of the indicator causes a memory protect interrupt to be sent to the CPU.

When a memory protect interrupt is received by the CPU, execution of the instruction is interrupted and a memory protect trap occurs indirectly through memory location SD.

3.4.1.4 Privileged Instruction Interrupt

The privileged instruction interrupt is an XPM option, available when the XPM is used with a model 4500-02 CPU. The XPM privileged CPU control function establishes two operating modes for the CPU, privileged and nonprivileged. In the privileged mode, all processor instructions are executable, while in the nonprivileged mode certain instructions can not be executed. Transition from one mode to another can occur under either interrupt control or program control. The privileged mode is invoked automatically following a power-up or system reset sequence, but can also be deliberately entered into under program control. The CPU is placed in the nonprivileged mode by the execution of a Load Status Register (LDS) instruction with bit 7 of the status word set.

An attempt to execute a privileged instruction while the CPU is in the nonprivileged mode results in a privileged instruction interrupt. Receipt of a privileged instruction is detected by the Privileged Instruction Detect logic. This logic then signals the Privileged and Memory Protect Interrupt Generator which generates an interrupt to notify the CPU.

When a privileged instruction error is detected by the CPU, a privileged instruction trap occurs. A No-Operation (NOP) instruction is executed in place of the instruction that caused the error. Next, an automatic BSP is executed to the location indicated by the contents of memory location $E. The processor P Register contents stored are always P+1, when P is the location of the first word of the instruction causing the error.

Execution of LDS when the CPU is in the nonprivileged mode does not affect the mode of the CPU, regardless of the state of bit 7 of the status word. However, when the CPU is in the privileged mode, execution of LDS prevents the next instruction executed from causing a privileged instruction trap.

3.4.2 External Interrupts

There are eight interrupt lines provided for the eight regular external interrupts. The external interrupt lines have the mnemonics INT08- thru INT15-, with interrupt line INT08- assigned highest priority and INT15- lowest. Interrupt line INT14- is reserved for the teleprinter, if standard GTE/IS software for the IS/1000 processor system is used.

The eight interrupt lines provided for external interrupts can be expanded to 16 using the XPM. The additional lines have the mnemonics INT00- thru INT07-, with interrupt line INT00- assigned highest priority and INT15- lowest. Interrupts 0 thru 7 are higher priority than interrupts 8 thru 15.

Each interrupt line can be used on an exclusive basis by a single peripheral device, or be commoned for use by up to 16 peripheral devices. When two or mare peripheral devices share a single interrupt line, they are considered as having a priority within a priority. Their priority is determined first by the relative priority of the common interrupt line and second, by the priority established for each peripheral device by the subroutine that services the common interrupt. This subroutine determines which peripheral device requires attention by issuing ICI and then examining the interrupt status word transferred to the A Register

Any combination of the external interrupts can be masked off by loading the N Register with ZEROs in the corresponding bit positions. The masked off interrupts are serviced when the mask is set again.

The external interrupts are asynchronous and may be activated by their respective controllers without regard to the state of any other controller or the CPU. Generally each controller has a flag that is set when the controller requires service. The flag is reset when the CPU has serviced the interrupt. The rate at which the interrupts may be processed depends upon the length of the subroutine required to process each interrupt and upon the delay for the CPU to recognize the interrupt. The CPU will recognize a pending interrupt after executing the current instruction, assuming that the instruction allows interrupts to occur after its execution. This

can introduce a delay of up to 10 us in the case of a Divide instruction, but normally varies from 0.75 us to 2.25 us for typical instructions.

3.4.2.1 Individual External Interrupt

Assuming that the machine is not in the Halt state but in either a Run or Wait state, then the operational logic of an individual external interrupt is sequenced as follows:

- The controller interrupt logic indicates to the CPU that it requires service by asynchronously turning on a flag which remains set until an appropriate response from the CPU has been received. This service may be a request for data transfer, an error condition, or the occurrence of an event like a switch transfer, relay closure, timer clock, etc.
- At spaced time intervals following the end of each instruction execution, the CPU priority logic examines the status of all interrupt lines. Since the interrupts are sampled at the conclusion of every instruction, an interrupt line must be held active long enough to be serviced. A pulsed interrupt request is not always serviced.
- The interrupt lines are ANDed with their corresponding N--Register bits and then sampled. The priority logic then selects the highest priority interrupt which is activated and is not masked out, i.e. disabled, by its corresponding N-Register bit. A simplified logic diagram of the flip-flops and logic involved per external interrupt level, is shown in Figure 3-4.
- In the event an interrupt is selected, the priority logic generates an address in memory for the interrupt location, places the selected interrupt in it and starts the interrupt control logic.
- If no interrupts are active, or the activated interrupts are masked out, no interrupt sequence occurs and a new instruction cycle is initiated.
- The information in the interrupt location corresponding to the priority selected interrupt, is fetched from memory. The contents of the memory location are used to address another location in memory into which the program counter is stored. The address is incremented by one and is then set into the program counter. During this hardware directed sequence, no sampling of the interrupt lines is allowed until the first instruction of the interrupt subroutine has been executed.
- At the end of each instruction of the subroutine, the interrupt logic looks for an interrupt of higher priority than the one currently selected. If no higher priority interrupt is detected, the interrupt servicing subroutine continues.

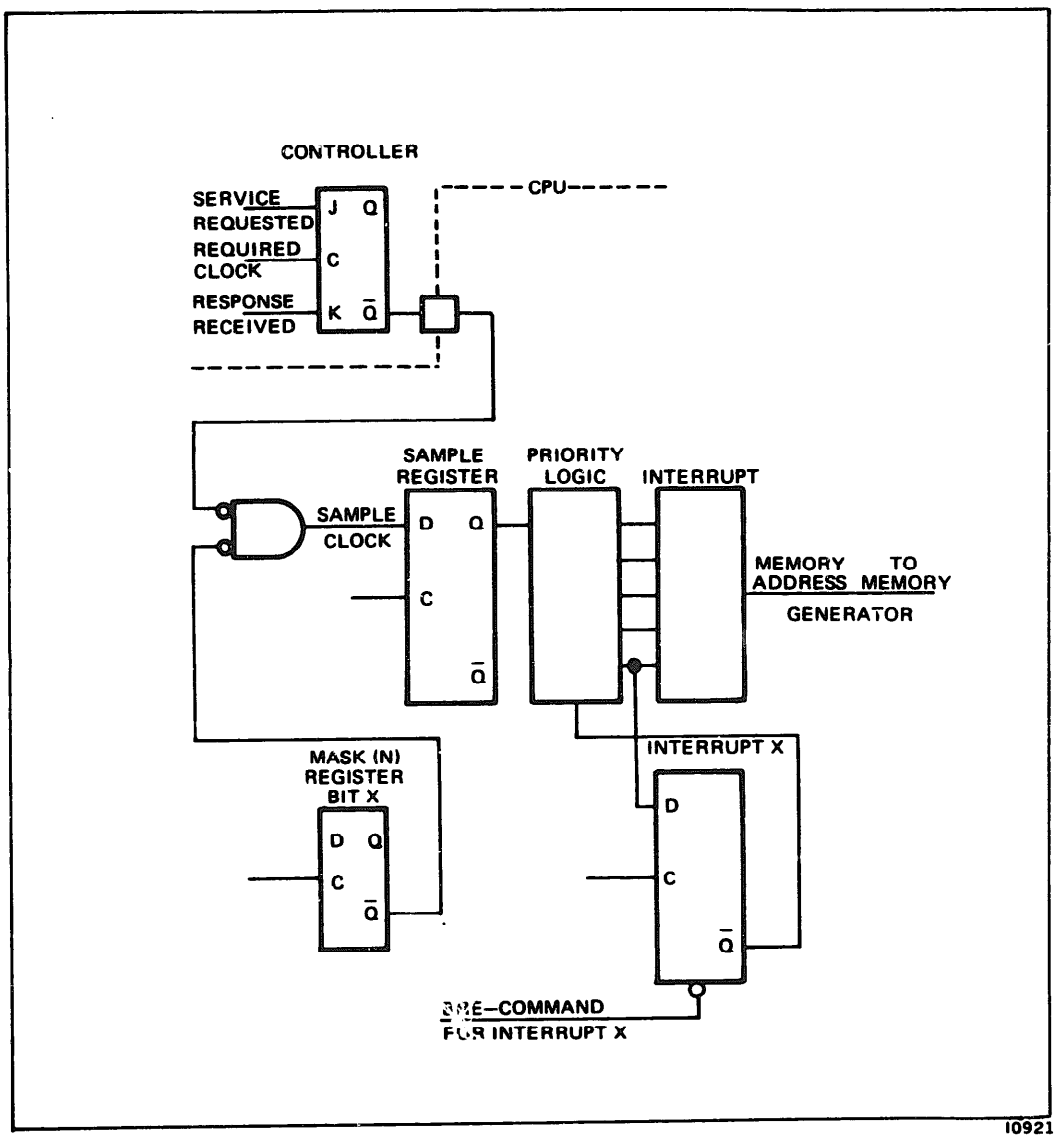


Figure 3-4. Simplified Logic for External Interrupts

- At some point in the interrupt subroutine the CPU sends a data input or output instruction to the controller. This resets the interrupt flip--flop in the controller but not the one in the CPU, and further processing of the interrupt may continue with interrupts to higher levels possible.
- The interrupt subroutine is concluded with an indirect BRE to the memory location where the old program counter is stored. Execution of the BRE resets the CPU interrupt flip-flop specified in the BRE, which should be that of the current interrupt.
- Control now returns to the interrupted program and the CPU continues processing from the point of interruption.

3.4.2.2 Common External Interrupts

The same hardware is used for individual interrupts as for common interrupts. However, in the common external interrupt logic scheme, the controller interrupt lines are ORed together. Therefore, any of the controllers can request service regardless of the state of the other controllers. The CPU samples the interrupt lines and selects the highest priority in the same manner, then calls in a basically identical subroutine to service the interrupt. The subroutine however, contains provisions that examine the state of the common interrupts so that the service request of the peripheral device with the highest priority, can be selected. ICI is used to bring the interrupt states of all controllers sharing the common interrupt line into the A Register. Generally, a test for negative and shift left loop is used to find the peripheral device with the highest priority.

As with the individual external interrupt, the servicing of a requesting controller resets the interrupt flip-flop in the controller, while the BRE terminating the subroutine resets the interrupt flip-flop in the CPU. If other common interrupts are pending, the interrupt flip-flop in the CPU is immediately set again at the completion of the BRE instruction, and is examined by the priority selection logic prior to the fetching of the next instruction.

3.5 DIRECT MEMORY ACCESS

The direct memory access (DMA) feature constitutes a channel through which data can be transferred using only one 750 ns memory cycle per word. This makes for a theoretical data transfer rate of 1.3 million words per second. However, due to inherent circuit delays, the practical data transfer rate must be set at approximately 1 million words per second. At data rates lower than 1 MHz, the DMA channel disconnects and frees the memory for processor controller access. DMA is an automatic function and can not be affected by an external program since there are no instructions controlling it. To use DMA, the program must condition the peripheral subsystem. If the power--fail-in-progress (PFIP) signal goes true, a controller can not request the DMA channel. If the PFIP signal goes true while the controller is using the DMA channel, the controller relinquishes the channel after completion of the current word transfer.

A peripheral subsystem requests DMA service by supplying the necessary control signals and its address information to the memory unit. An optional IOP is available to simplify use of the DMA function. The IOP supplies the control signals and sequences the memory address for all standard peripheral devices. See Table 3-2 for definition of mnemonics pertinent to the DMA logic.

3.5.1 DMA Selection Sequences

When the controller requires a DMA service cycle, the outgoing DMA priority line assigned is made low. The controller waits for its incoming priority line and the DMRQ line to go high, which signifies

Table 3-2. DMA Mnemonics

Mnemonics	Definition
DMALD-	The Address Load or Data Load Enable is used to gate address and data bits 00 thru 15 via the I/O interface to the memory. This signal must be low to send data or address to the memory and high when expecting to receive data from the memory.
DMRQ-	The DMA Request Line is used to request a DMA cycle. DMRQ should not be issued until the DMA response line (DMRS) is not busy because two DMA devices can not use the DMA channel simultaneously.
DMRS-	The DMA Response Line is used to determine if the DMA is in use.
BUSY+	This response (when low) from the memory indicates that the memory will accept a new memory address. As soon as this line falls, a memory start (DMAMS) may be given.
DMAMS-	The DMA Memory Start is used to initiate a memory cycle. DMAMS strobes the memory address into the memory address register on its negative going edge.
DMACW0-	This signal is used when writing data into the most-significant eight bits of memory. (Bits 00 thru 07.) When reading from memory this signal is not activated.
DMACW1-	This signal is used when writing data into the least--significant eight bits of memory. (Bits 08 thru 15.) When reading from memory this signal is not activated.
DMAST-	The Data-In Strobe is used to strobe data bits 00 thru 15 into the memory.
DMOS-	The Data-Out Signal is used to indicate that the data will soon be ready on the I/O bus. The data should not be sampled before 150 ns after the DMOS signal is received.
DIB00- thru DIB15-	The input data bus is used to transfer address bits 00 thru 15 to the memory address register and transfer data bits 00 thru 15 to the memory data register.
DOB00- thru DOB15-	Output da - bus bits 00 thru 15 are used to transfer data to the DMA device from the memory data register.
PFFIP-	This signal indicates that a Power Failure/Restart cycle is in progress. Therefore, a DMA operation must be terminated at the completion of the current memory cycle to allow the CPU to have an orderly shutdown, or startup.
DMAP1- thru DMAP3-	DMA Priority Determinations: These signals are used to establish priority for allocation of the DMA facility to contending external DMA controllers. The priority determination is done completely within the DMA controllers and the CPU has no control as to how these lines are used. The DMA priority signal originates from one controller and is received by a single lower priority controller which in turn repowers the signal and retransmits it over another DMAPX line to a still lower priority controller, if one exists.

that the DMA channel is not busy and no higher priority controller requires the DMA channel. The controller then requests the use of the DMA channel by causing the DMRQ line to go low. Simultaneously, the controller starts a 210 ns time delay, at the conclusion of which the controller samples its incoming DMA priority line to determine whether any other device of higher priority is requesting use of the DMA channel. If a higher priority device requires ser.. vice, the controller must cancel its DMA request by allowing term DMRQ to go high and wait until its priority line goes high once more before making another DMA request.

If no higher priority device requires service and term DMRS is still true as the 210 ns times out, the controller claims the DMA channel by placing the memory address on the DIB lines (DIB00 thru DIB15). The controller can initiate one memory transfer, in or out of memory, by bringing up term DMAMS (DMA Memory Start), minimally 415 ns after the address has been placed on the bus if BUSY is low. If BUSY is high, the controller must wait until BUSY goes low. The DMAMS pulse must be within the boundaries of 150 ±100 ns.

At the conclusion of each memory transfer, the controller checks its incoming DMA priority line to determine whether a higher priority device requires the DMA channel. If a higher priority device needs DMA, the controller releases the DMA channel to the higher priority device. After the higher priority device has completed its data transfers, the controller can resume its data exchange by entering another DMA request.

3.5.2 DMA Transfer into Memory

If data is to be transferred into the memory, the clear/write flags, terms DMACWO and/or DMACW1 must be brought up within 50 ns of the leading edge of DMAMS and remain stable for 500 ±100 ns. (Figure 3-5).

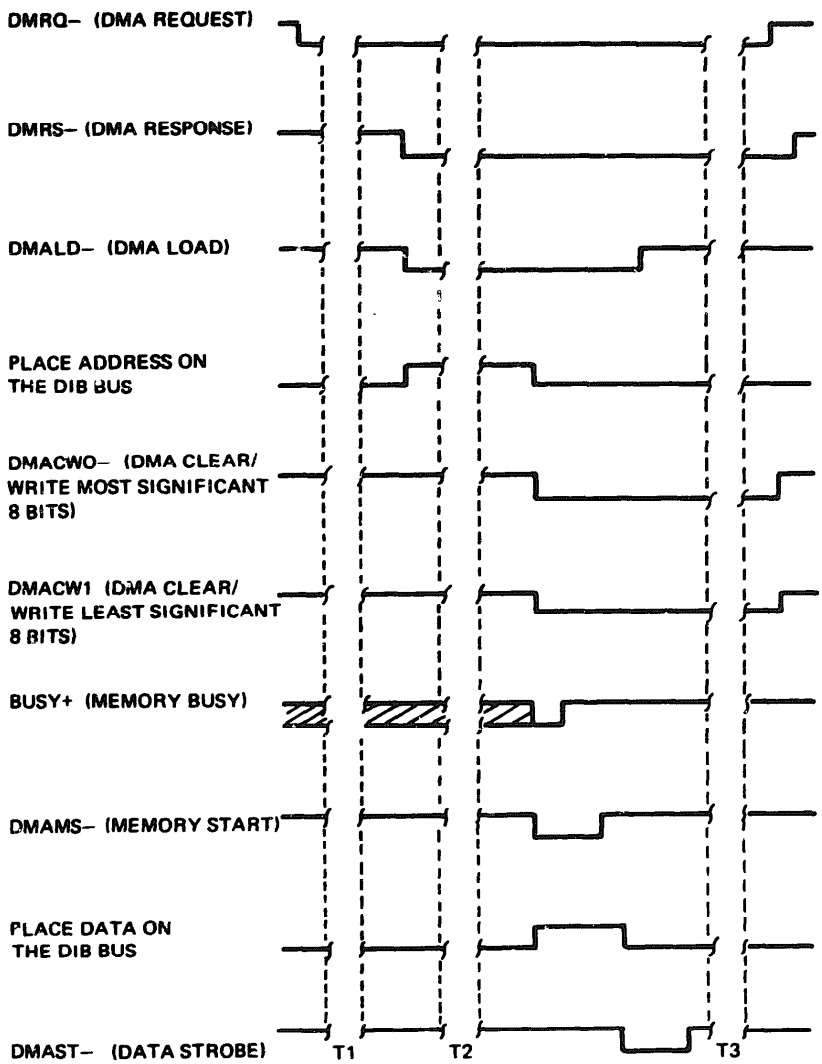
The data strobe, DMAST, must be sent a maximum of 240 ns after the leading edge of DMAMS. The data to be stored in the memory must be on the DIB lines at least 100 ns before DMAST is transmitted. The DMAST strobe pulse must be 150 ±100 ns wide. Term DMALD+ must remain true for the duration of the address and data transfers.

3.5.3 DMA Transfer out of Memory

Data from the memory data register is preceded by term DMOS to ready the controllers for reception of the data. The data at the perip- heral device must be stable for 150 ns after the leading edge of term DMOS and remain stable until another memory cycle is initiated by either the CPU or the DMA controller. (Figure 3-6.)

3.5.4 DMA Single and Multiple Cycle Determination

If a single DMA cycle is desired, term DMRQ must be dropped after the leading edge of term DMAST during a write operation, and as soon as the data has been read out during a read operation. I f multiple cycles are desired, term DMRQ must remain active.



T1 WAIT FOR THE DMA RESPONSE TO THE DMA REQUEST.

T2 WAIT FOR THE "AND" OF THE FOLLOWING TWO CONDITIONS BEFORE SENDING MEMORY START (DMAMS–).
A. MEMORY NOT BUSY (I.E., BUSY+ IN A LOW STATE).
B. THE DMA MEMORY ADDRESS HAS BEEN ON THE DIB BUS AT LEAST 415 NANOSECONDS'.

T3 WAIT FOR THE CLEAR/WRITE SIGNALS TO TIME OUT (DMACW0– AND/OR DMACW1– MUST REMAIN LOW FOR 500 NANOSECONDS AFTER MEMORY START, DMAMS–, GOES LOW).

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Figure 3-5. Write Operation Timing Diagram

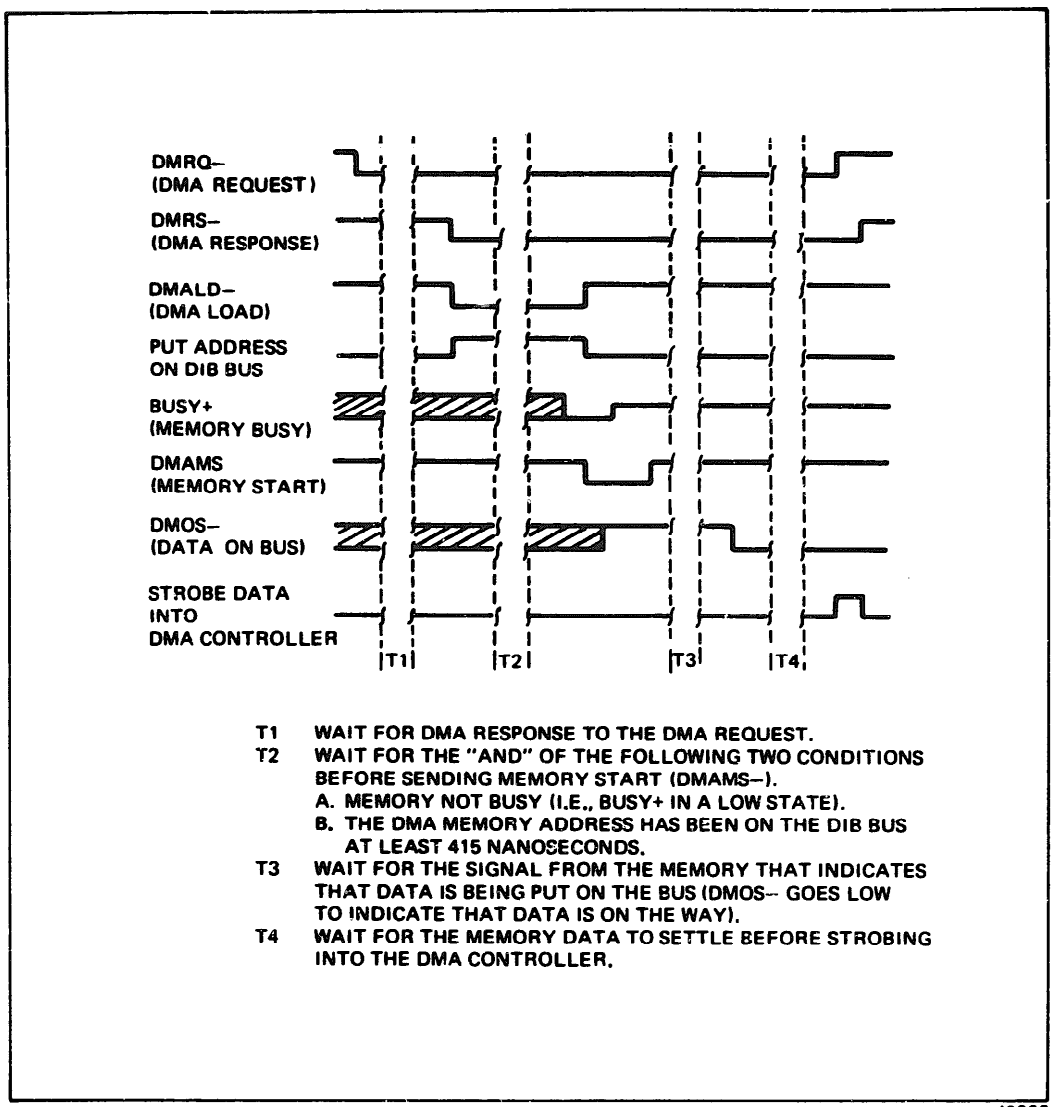


Figure 3-6. DMA Read Operation Timing Diagram

3.5.5 DMA Control Priority Determination

Before a DMA cycle can be executed, the DMA controller must obtain control of the DMA channel. The logic used for the control function is shown in Figure 3-7.

Term DMAND+ (DMA need) indicates to the controller that a DMA cycle is needed. Term PFFIP- (power fail function in progress) is sent from the CPU when the power fail/restart interrupt function requires service. Terms DMAND and PFFIP are input to NAND gate A; the output, term DMRQD- (DMA required) is propagated as the outgoing DMA priority line. The selection of the outgoing priority lines DMAP1, DMAP2 or DMAP3, is determined by a patch at IC socket D. The selected priority line informs all lower priority devices to release the DMA channel upon completion of their current memory cycle and to refrain from requesting the DMA channel until the priority line goes high again. The incoming priority line (DMAENB+) is also selected at patch D.

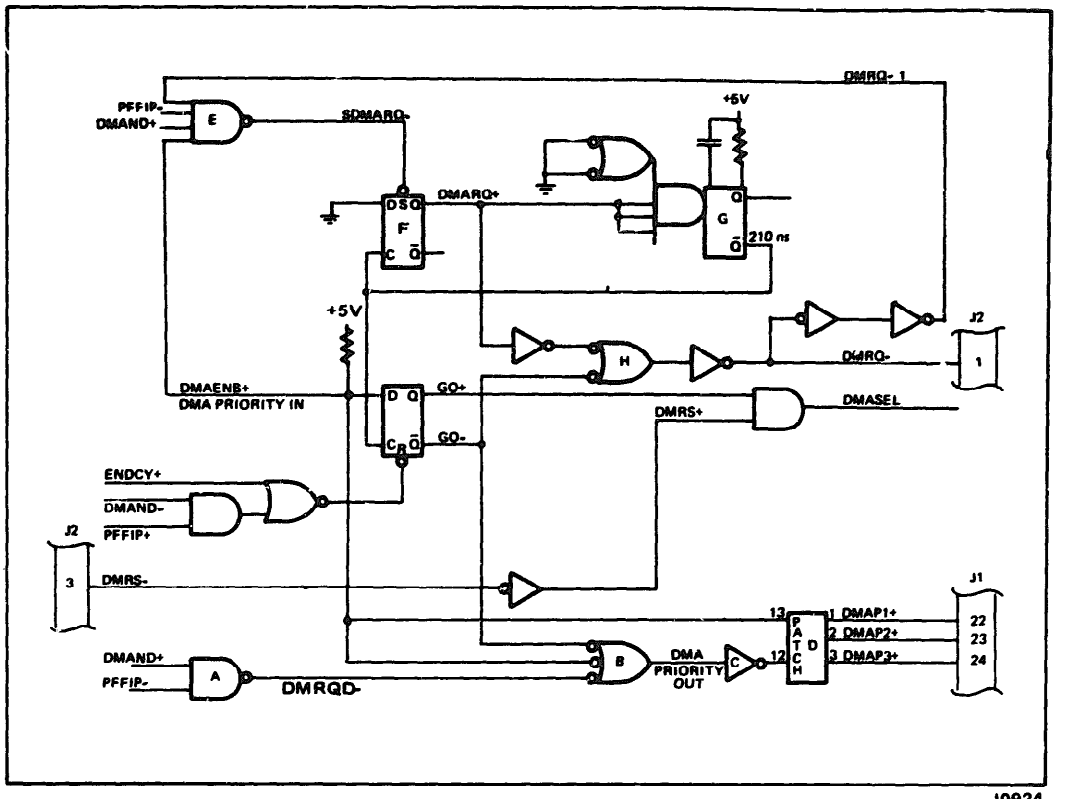


Figure 3-7. DMA Priority Determination Logic

When the inputs to NAND gate E, terms DMAND+, DMRQ-1 (DMA Request signal buffered) and DMAENB+ (DMA priority in), are all high, output term SDMARQ- will go true, which starts the DMA request sequence.

Term SDMARQ- going low sets flip-flop F, which in turn fires the 210 ns one-shot G. The 210 ns is used to allow the DMA priority lines to propagate through the entire I/O bus in the event that several devices are requesting the DMA channel simultaneously. When the one-shot times out, its $\overline{Q}$ output resets the F flip-flop and clocks the GO flip-flop to a set or reset condition, depending upon the logical state of term DMAENB.

If the GO flip-flop is reset, the DMRQ- line will be released and the higher priority device will claim the DMA channel. Another DMA cycle can be requested as soon as the incoming priority line goes high and term DMRQ- goes high. If the GO flip-flop is set, term DMRQ- will be held low through gate H from GO- and the controller can proceed with its DMA cycle. At the end of the DMA cycle the reset of GO allows DMRQ- to go high and releases the DMA facility. Every controller releases the DMA facility when a higher priority DMA device requests the channel or when PFFIP goes low, however, the timing criteria vary from one controller to another.

If a higher priority device signals over the DMA priority lines that it needs the DMA channel, term ENDCY+ (end cycle) is generated to reset the GO flip-flop. This causes term DMRQ- to go high, which

releases the DMA channel. Term ENDCY+ remains low if the controller has continuous need for the DMA channel, provided no higher priority device is requesting the DMA channel.

The Q-output of the GO flip-flop, when active, is communicated via the priority line to all controllers of lower priority, to indicate that a DMA cycle is in progress. Transmission of the signal is necessary because in expanded systems, term DMRQ- being undirectional, will appear to be high in some chassis while it may be low in another expansion chassis. The priority network will indicate the channel is in use to all lower priority devices, DMRQ- indicates this to all higher priority devices.

SECTION 4
PROGRAMMING CONSIDERATIONS

4.1 GENERAL

All input and output transfers of data between the CRU and peripheral device controllers (except DMA) are executed under program control. The following five Basic I/O instructions control the input and output operations:

- EDF: Execute Device Function.
- ICI: Interrogate Common Interrupts.
- RDS: Request Device Status.
- WTI: Word Transfer In, i.e., peripheral subsystem to CPU.
- WTO: Word Transfer Out, i.e., CPU to peripheral subsystem.

The following four instructions control the priority interrupt function:

- BRE: Branch and Reset External Interrupt.
- BRI: Branch and Reset Internal Interrupt.
- LIE: Load Interrupt Enable (N) Register.
- SIE: Store Interrupt Enable (N) Register.

4.2 INSTRUCTIONS

4.2.1 I/O Instruction

The five I/O instructions, EDF, ICI, RDI, WTI and WTO, all have the format shown in Figure 4-1. The C-field for all I/O instructions is 0010.

4.2.1.1 EDF Instruction

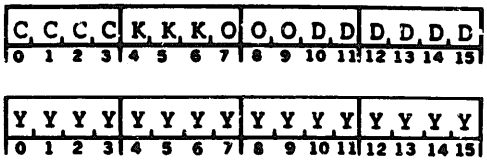
EDF D,Y,O

D = device address.
Y = address of branch on instruction reject.
0 = order line code.

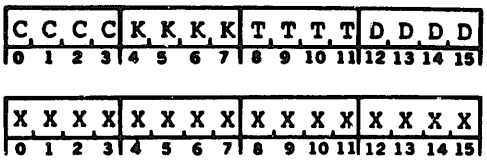
The action specified by the order line code is performed by the addressed controller. Generally, there is a different set of EDF instructions for each controller in the configuration, although certain functions are common to most controllers (start read, start write, etc.).

If the three order code bits are not sufficient to specify all functions that must be performed by a controller, the contents of the A Register are available for further coding. The A Register may be used to contain data or an address required to perform the function, i.e., the starting address for a drum memory.

I/O Instruction



Interrupt Instruction



C = instruction type: 0010 for I/O instructions.
0100 for interrupt instructions

K = instruction class, as follows:

Bit 4	Bit 5	Bit 6	Bit 7	Instruction
0	0	0	N/A	EDF
0	0	1	N/A	WTO
0	1	0	N/A	WTI
0	1	1	N/A	RDS
1	0	0	N/A	ICI
1	0	1	N/A	Spare
1	1	0	N/A	Spare
1	1	1	N/A	Spare
0	0	1	0	LIE
0	0	1	1	SIE
1	0	0	0	BRI
1	0	0	1	BRE

I/O instructions:
O = order line code. For the EDF instruction, the code specifies a particular function to be performed by the external device, i.e., read, write, set mode, etc For I/O instructions other than EDF, the order code can be used for special decoding at the controller level.

D = device address.

Y = reject address.

Interrupt instructions:
T = addressing mode.

D = register needed by T or flip-flop to be reset.

Y = operand address.

Figure 4-1. Instruction Format

4.2.1.2 ICI Instruction

ICI, D,Y

D = device address.

Y = address of branch on instruction reject.

Controller logic is designed so that the controller does not echo during ICI even though the instruction contains the correct device address, unless that controller actually has an interrupt pending and therefore requires common interrupt service.

NOTE: Those devices that do not share a common interrupt should also be disabled from responding to ICI even if they have the correct address and an interrupt pending.

Since up to 16 controllers can share a common interrupt line, ICI is provided to determine which controller(s) activated the interrupt. After execution of ICI, the contents of the A Register are examined. Each controller on the common interrupt line is assigned a different A-Register bit with which to report its interrupt status. Although it is a function of the software, the common interrupt line priority normally established is that the controller corresponding to bit position 0 has highest priority, and the controller corresponding to bit position 15 has lowest priority.

Up to four common interrupt lines can be used. The two most-significant bits of the ICI device address specify the common interrupt line. The device address of every controller on a particular common interrupt line must have the same two most-significant bits. In the case of a controller with more than one device address, any device address not used by a controller on a common interrupt line can be used by a controller on an individual interrupt line. In the case of a controller with two or more interrupts, but only one device address, the same device address may be used on both the individual and common interrupt lines.

4.2.1.3 RDS Instruction

RDS, D,Y

D = device address.

Y = address of branch on instruction reject.

The status word of the addressed controller is transferred to the A Register for examination.

The status word provides information about the current status of the controller, such as: whether or not it is ready to respond, whether or not an error has occurred, and, if so, what type, what operational mode is in effect, etc.

4.2.1.4. WTI Instruction

WTI, D,Y

D = device address.

Y = address of branch on instruction reject.

One data word is transferred from the addressed controller to the A Register.

4.2.1.5 WTO Instruction

TO, D,Y

D - device address.

Y = address of branch on instruction reject.

One data word is transferred from the A Register to the addressed controller.

4.2.2 Interrupt Instructions

The four interrupt instructions, BRE, BRI, LIE AND SIE, all have the format shown in Figure 4-1. The C-field for all instructions is 0100.

4.2.2.1 BRE Instruction

BRE T,D,Y

T = addressing modes for the BRE instruction (see GTE/IS manual E0006 for description of addressing modes.

D = external interrupt flip-flop to be reset.

The specified CPU external interrupt flip-flop is reset and address Y is used in setting the P Register. The value that goes into the P Register is a function of the addressing mode specified by T-field bits 8 thru 11.

4.2.2.2 BRI Instruction

BRI T,D,Y

T = addressing modes for the BRI instruction (see GTE/IS manual E0006 for a description of addressing modes).

D = internal CPU interrupt flip-flop to be reset.

Y = branch address.

The specified CPU internal interrupt flip-flop is reset and Y is used in setting the P Register. The value that goes into the P Register is a function of the addressing mode specified by T-field bits 8 thru 11.

4.2.2.3 LIE Instruction

LIE T,D,Y

T - addressing modes for the LIE instruction. (See GTE/IS manual E0006 for a description of addressing modes).

D = register that may be needed by the addressing mode.

Y = operand address.

The N Register is loaded with the contents of the effective memory location determined by T, D and Y.

The N Register enables and disables external interrupts under program control. Each bit position of the N Register corresponds to the external interrupt line with the same number.

Disabling an interrupt line (N-Register bit = ZERO) does not affect the interrupt line status, but does prevent the interrupt from being recognized. The interrupt line may be set while it is disabled and it will be processed when it is again enabled.

4.2.2.4 SIE Instruction

SIE T,D,Y

T = addressing modes for the SIE instruction (See GTE/IS manual E0006 for a description of addressing modes).

D = register that may be needed by the addressing mode.

Y = operand address.

The contents of the N Register are stored in effective memory location Y. The N Register is eight bits wide, therefore only eight bits (08 thru 15) of the word stored in memory correspond to the N Register. Because the N Register is only eight bits wide, the data stored in locations 0 thru 7 has no meaning and is undefined.

SECTION 5
APPLICATIONS

5.1 GENERAL

This section serves to aid the systems user in implementing the functional and electrical requirements of interface design, and in applying the programming information given in the previous section.

Paragraph 5.2 describes the operational criteria for a high-speed paper tape (HSPT) controller interface, and gives a sample input/output program for use with a HSPT reader/punch. The HSPT controller interface was chosen as an input/output interface example because of its common use and its requirements which are similar to any controllers.

Paragraph 5.3 describes two examples of interrupt subroutines. While both subroutines are hypothetical, they are representative of the subroutines commonly in use.

5.2 HIGH SPEED PAPER TAPE INTERFACE

5.2.1 General Description

The HSPT controller provides a program controlled interface between the CPU and a combined 400-character per second reader and 120-character per second punch.

Data transfers are byte oriented, with reader data transferred to the least-significant eight bits of the A Register and punch data transferred from the most-significant eight bits of the A Register.

5.2.2 Program or Internal Control

The HSPT reader/punch has one device address and one interrupt line for its reader station and its punch station. Table 5-1 defines all instructions accepted by the controller. Table 5-2 lists all conditions under which reader and punch interrupts are turned on and off in the controller.

5.2.2.1 Input Control

Paper tape can be read continuously or one character at a time. If the tape is to be read continuously, the input operation can either be started through EDF RDC with the first character to reach the read station, or through EDF RSL with the first nonzero character to be detected. If WTI is not received in time, the paper tape stops

Table 5-1. HSPT Controller Instruction Set

Name	Mnemonic	Description
Word Transfer In	WTI	One byte is transferred from the reader to A-Register bits 8 thru 15.
Word Transfer Out	WTO	One byte is transferred from A-Register bits 0 thru 7 to the punch.
Read Device Status	RDS	The controller status word is transferred to the A Register for examination.
Interrogate Common Interrupts	ICI	The interrupt status of controllers that share a common interrupt line is transferred to the A-Register for examination.
Execute Device Function, Read One Character	EDF ROC	The reader advances one character position, reads the character and generates an interrupt.
Execute Device Function, Read Continuously	EDF RDC	The reader advances one character position, reads the character, generates an interrupt and repeats the sequence (up to 400 times per second).
Execute Device Function, Read Skipping Leader	EDF RSL	Executes the same as EDF RDC except that blank leader is skipped before the controller begins generating interrupts.
Execute Device Function, Stop Read	EDF STP	The reader halts immediately with the controller in the idle state.
Execute Device Function, Write Continuously	EDF WRC	The punch generates an interrupt for data, advances one character position, punches the data and repeats the sequence (up to 120 times per second).
Execute Device Function, Punch Leader	EDF PUL	The punch punches 192 sprocket holes with no data.
Execute Device Function, Stop Write	EDF SWR	The punch halts immediately with the controller in the idle state.

Table 5-2. HSPT Controller Interrupt Conditions

On Conditions	Off Conditions
Reader	
Detection of a character after EDF ROC starts the reader.	Receipt of WTI.
Detection of each character after EDF RDC or EDF RSL starts the reader.	Receipt of WTI. (Receipt EDF STP stops the reader.)
Punch	
Start of tape motion before a character is punched as a result of EDF WRC.	Receipt of WTO.

on the next character and waits for WTI without losing that character. However, if a EDF STP is given after the tape has stopped without first executing WTI, the character will be lost.

5.2.2.2 Output Control

The execution of EDF WRC causes the paper to be punched continuously until stopped by EDF SWR. Continuous output operation is effected.

A length of 19.2 inches of paper tape can be punched with sprocket holes for the leader or trailer segments of the tape, by using EDF PUL. If no WTO has been received at the end of the sprocket hole punching operation, the punch stops and assumes a Wait state.

5.2.2.3 Input/Output Control

The HSPT reader and punch may be operated separately or concurrently. To operate them concurrently while they share the same interrupt line, ICI must be executed to determine which device is requesting service. When an interrupt occurs, ICI is executed and the contents of the A Register examined. If bit position 0 contains a ONE, the reader is requesting service; if bit position 1 contains a ONE, the punch is requesting service. Concurrent operation of the reader and punch does not reduce the data rate of either device.

5.2.2.4 Status Control

Both a reader status and a punch status are generated and available. RDS with an order line code of zero transfers the reader status into the A Register. RDS with an order line code of one transfers the punch status into the A Register.

5.2.3 Operator or External Control

When the operator presses the control panel RESET switch, the HSPT is placed in an idle state. This is comparable to execution of EDF STP or EDF SWR under internal or program control. External control overrides internal control at all times.

5.2.4 Sample Program

This sample program represents a hypothetical interrupt subroutine to read a block of data into a memory buffer. The major segments of the subroutine are separated by spaces in the listing for clarity.

Few changes are required to convert the example to an actual output subroutine. Little additional coding would be required to make the subroutine handle input and output transfers, or to handle a common interrupt.

5.2.4.1 Program Listing

Label	Command	Operand	Comments
START	LDA	CONST1	Load initial character count.
	STA	CCOUNT	Store initial character count.
	LDA	CONST2	Load initial buffer index.
	STA	INDEX	Store initial buffer index.
	EDF		Read continuous.
*			(Wait for interrupt)
INIT	CON	0	Interrupt recognized, control transferred to subroutine.
	STA	SAVEA	Save contents of working register A.
	STB	SAVEB	Save contents of working register B.
WRT	LDB	INDEX	Fetch buffer index.
	WTI		Transfer a word.
	STA	BUFFER,B	Store the word in the buffer.
	IRT	B,B	Increment and replace B.
	STI	INDEX	Replace buffer index.
COUNT	LDA	CCOUNT	Fetch character count.
	DRT	A,A	Decrement and replace A.
	BAR	STOPE	Branch if character count is zero.
	STA	CCOUNT	Replace character count.

Label	Command	Operand	Comments
COMP	LDA	SAVEA	Replace contents of working register.
	LDB	SAVEB	Replace contents of working register.
	BRE	INIT,I	Return control to main program.
STOP	EDF		Stop reader.
	BUR	COMP	Branch to completion segment
SAVEA	CON	0	Space for working register.
SAVEB	CON	0	Space for working register.
INDEX	CON	CONST2	
CCOUNT	CON	CONST1	
CONST1	CON	VALUE1	Initial character count = Value 1.
CONST2	CON	VALUE2	Initial buffer index = Value 2.
BUFFER	CON	0	Starting location of data buffer.
			Rest of buffer.
	CON	0	

5.2.4.2 Program Description

START span turns on the reader, and initializes the character count and index values. When the reader detects the first character, an interrupt is generated.

INIT initializes the processor for a word transfer by saving the contents of registers that will be used in subsequent segments. This segment is entered by the branch instruction at the hardwired interrupt trap location. The old P-Register value is stored in the first location INIT.

WTR effects a word transfer into a data buffer. A different buffer can be used by changing the index value prior to starting the reader. With simple changes, this could become a word-transfer out segment.

COUNT institutes the character count monitor. The count of characters left in the block is decremented and checked for zero value. If zero characters are left, the block transfer is over and a branch instruction is executed to STOP. If additional words are to be transferred, the subroutine goes to COMP. A different length block can be specified by changing the character count value prior to starting the reader.

STOP stops the reader and branches, to COMP to exit the subroutine.

COMP completes processing of the interrupt by restoring the original contents of working registers and executing a BRE thru INT (to pick up the old P-Register value). Once the interrupt is reset, the main program can continue processing until another reader interrupt is recognized.

SAVEA and SAVEB create spaces for constants and working subroutine storage.

Buffer constitutes the starting location of the data buffer.

5.3 INTERRUPT PROGRAMMING

5.3.1 General

Typical I/O interrupt subroutines that enable processing between interrupts are presented in this paragraph. One subroutine uses the X Registers, the second does not. Generation and processing of the EKO interrupt recognition signal is also described.

5.3.2 Sample Program 1

This sample program represents a hypothetical subroutine for processing between interrupts, using the X Registers. The following conditions are assumed to be in effect:

- The CPU is processing when the interrupt occurs (i.e., CPU status must be stored and reloaded).
- The output table address and table length have been given in the I/O subroutine calling sequence and saved by the I/O subroutine initialization.
- The interrupt mask is set to enable the interrupt.
- EDP has been executed to start the output device.
- The interrupt is processed as soon as it is set (no latency time).
- Three X Registers (X2, X3 and X4) are dedicated to this interrupt.

5.3.2.1 Program Listing

Label	Instruction	Operand	Comments	Cycles
	BSP (Simulated)	INT		2.0
INT	CON	0		
	TRF	A, 2	Save A Register	1.0
	LDA	0, X, 3	Fetch Output Data	3.0
	WTO	DEV, REJECT	Output	1.5
	IRT	3, 3	Increment Index	1.0
	IRT	4, 4	Increment Table Length	1.0
	BIR	E, DONE	If Output Complete, Branch	1.0
CONT	TRF	2, A	Restore A Register	1.0
	BRE	DEV, INT, I	Return to Caller	3.0
				14.5
DONE	BSP	TERM	Call Terminate Routine	*
	BAR	GE, CONT	If Terminate, Continue	*
	EDG	DEV, REJECT	Stop I/O	*
	BUR	CONT		*

5.3.3 Sample Program 2

This sample program represents a hypothetical subroutine for processing between interrupts without the use of X Registers. The following conditions are assumed to be in effect:

- The CPU is processing when the interrupt occurs (i.e., CPU status must be stored and reloaded).
- The output table address and table length have been given in the I/O subroutine calling sequence and saved by the I/O subroutine initialization.
- The interrupt mask is set to enable the interrupt.
- EDF has been executed to start the output device.
- The interrupt is processed as soon as it is set (no latency time).
- Throughput is approximately 77,000 words per second.

*Terminate branch only

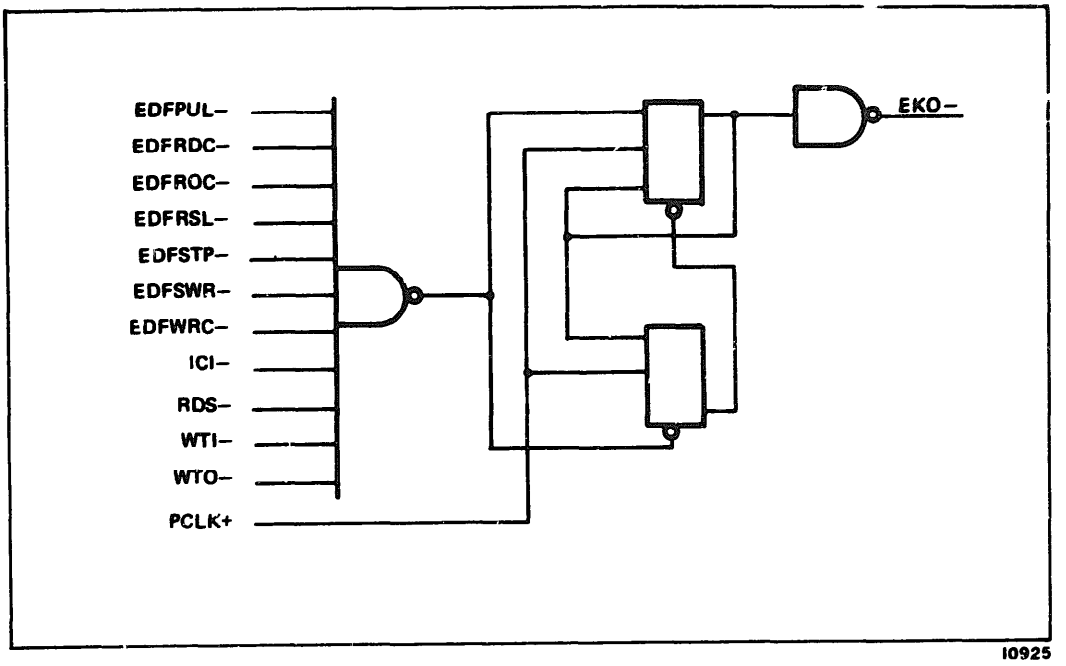


Figure 5-1. HSPT Controller EKO Logic (Simplified)

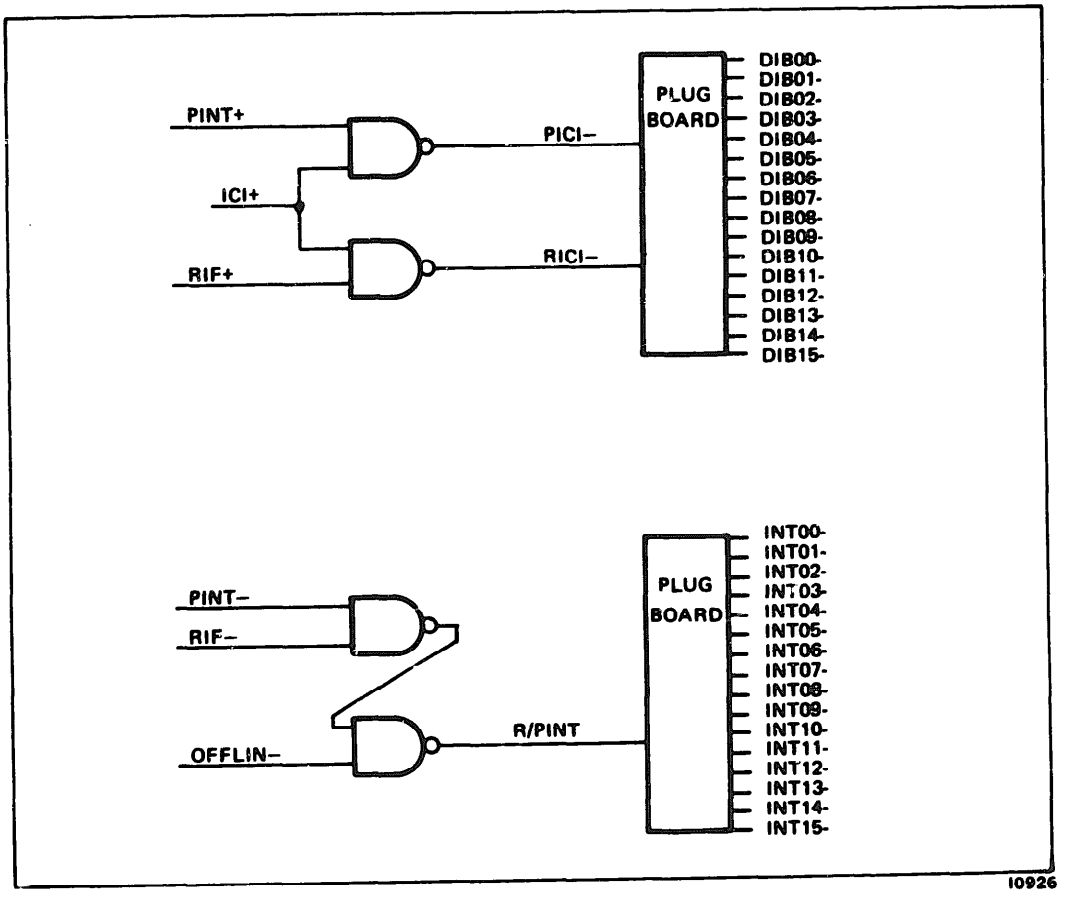


Figure 5-2. HSPT Controller Interrupt Logic (Simplified)

APPENDIX A
ASSIGNED I/O INSTRUCTION CODES

This appendix lists reserved instruction codes for special and general I/O operations. Refer to the appropriate maintenance manual for I/O instruction codes of specific devices.

Table A-1. Special Operations

Computer Operation	Device Code 0 thru 15	Device Code 16 thru 31	Device Code 32 thru 47	Device Code 48 thru 63
ICF	21CE			
RIS	264E			
SYC	2B0N	2B1N	2B2N	2B3N
SYR	2A0N	2A1N	2A2N	2A3N

Notes:

- N represents 0 thru 15 ($0 thru $F) device code
- Second word of instruction contains address of branch on reject

Table A-2. General I/O Operations

Computer Operation	Device Code 0 thru 15	Device Code 16 thru 31	Device Code 32 thru 47	Device Code 48 thru 63
EDF	200N	201N	202N	203N
ICI	280N	281N	282N	283N
RDS	260N	261N	262N	263N
WTI	240N	241N	242N	243N
WTO	220N	221N	222N	223N

Notes:

- N represents 0 thru 15 ($0 thru $F) device code
- Second word of instruction contains address of branch on reject

APPENDIX B
WORK FORMATS

B.1 GENERAL

Various processor instructions cause the transfer of data (words) either within the CPU or between the processor and a device controller. This appendix includes the following tables which contain descriptions of the word formats used by the processor and device controllers:

Table	Title
B-1	IS/1000 Processor
B-2	Type 1 Expanded Performance Module
B-3	Type 2 Expanded Performance Module
B-4	High Capacity Removable Disc Controller
B-5	Medium Capacity Removable Disc Controller
B-6	Rotating Drum Memory Controller
B-7	Asynchronous Modem Multiplexer
B-8	Asynchronous Communication Adapter
B-9	Synchronous Modem Multiplexer
B-10	Synchronous Communication Adapter
B-11	Automatic Calling Unit Multiplexer
B-12	Block Check Unit
B-13	Communication Transfer Unit
B-14	System Control Unit
B-15	Terminal Control Channel Interface Unit
B-16	Tape Unit Channel Interface Unit
B-17	Input/Output Processor:
B-18	Nigh Speed Paper Tape Reader/Punch Controller
B-19	Card Reader/Line Printer Controller
B-20	Standard Card Punch Controller
B-21	Universal Magnetic Tape Controller
B-22	Utility Controller and Distributor and Utility Controller

Each table contains a list of all the instructions (for a given unit) that cause the transfer of a word. For each instruction, the word involved is described in terms of the CPU register affected.

Table B-1. IS/1000 Processor (Sheet 1 of 3)

Instruction	Register		
	Name	Bit	Meaning
LDS: Load Status (S) Register	S	7*	Nonprivileged mode indicator: 0 = privileged mode. 1 = nonprivileged mode.
		8	Less than.
		9	Greater than.
		10	Equal to.
		11	Overflow.
		12	Program flag 8.
		13	Program flag 4.
		14	Program flag 2.
		15	Program flag 1.
STS: Store Status (S) Register	S	7 thru 15	Same as LDS.
LIE: Load Interrupt Enable (N) Register	N	8 thru 15	ONE in any bit position enables the corresponding external interrupt line.
SIE: Store Interrupt Enable (N) Register	N	8 thru 15	Same as LIE.
LAB: Load A-Register Byte, Index X Register	X	0 thru 14	Operand address index.
		15	Byte: 0 = upper byte (bits 0 thru 7) of effective address. 1 = lower byte (bits 8 thru 15) of effective address.
SAB: Store A-Register Byte, Index X Register	X	0 thru 15	Same as LAB.
LBB: Load B-Register Byte, Index X Register	X	0 thru 15	Same as LAB.
SBB: Store B-Register Byte, Index X Register	X	0 thru 15	Same as LAB.
MUL: Multiply Memory by B Register**	A	0	Sign
		1 thru 15	Most-significant bits of product.

*XPM option, available only on 4500-02 CPU
**Optional, for use with Multiply/Divide Option

Table B-1. IS/1000 Processor (Sheet 2 of 3)

Instruction	Register		
	Name	Bit	Meaning
	B	0	Reset to ZERO
		1 thru 15	Least-significant bits of product.
DIV: Divide A and B Registers by Memory**			AT START OF DIVISION:
	A	0	Sign.
		1 thru 15	Most-significant bits of dividend.
	B	0	Not part of dividend.
		1 thru 15	Least-significant bits of dividend.
			AFTER DIVISION:
	B	0 thru 15	Quotient.
	A	0 thru 15	Remainder.
INC: Increment Memory and Compare with Zero	S	8 thru 11	Same as LDS.
CAM: Compare A Register with Memory	S	8 thru 10	Same as LDS.
CBM: Compare B Register with Memory	S	8 thru 10	Same as LDS.
CXM: Compare X Register with Memory	S	8 thru 10	Same as LDS.
CRR: Compare Register 1 with Register 2	S	8 thru 10	Same as LDS.
RPF: Reset Program Flags	S	11 thru 15	Same as LDS.
SPF: Set Program Flags	S	11 thru 15	Same as LDS.
EDF, WTI, WTO, RDS and ICI	A	0 thru 15 as req'd	Refer to Tables B-2 thru B-22.
ICF: Internal Control Function	A	3, 4	Instruction trap interrupt.
		5, 6*	Memory protect interrupt.

*XPM option, available only on 4500-02 CPU
**Optional, for use with Multiply/Divide Option

Table B-1. IS/1000 Processor (Sheet 3 of 3)

Instruction	Register		
	Name	Bit	Meaning
RIS: Request Internal State	A	7, 8*	Privileged instruction interrupt.
		10*	Privileged instruction interrupt latch.
		0	Power fail state.
		3, 4	Instruction trap interrupt.
		5, 6*	Memory protect interrupt.
		7*	Privileged instruction interrupt.
		10*	Privileged instruction interrupt latch.
*XPM option, available only on 4500-02 CPU			

Table B-2. Type 1 Expanded Performance Module

Instruction	Register		
	Name	Bit	Meaning
LDS: Load Status (S) Register	S	7	Nonprivileged mode indicator: 0 = privileged mode. 1 = nonprivileged mode.
		8	Less than.
		9	Greater than.
		10	Equal to.
		11	Overflow.
		12	Program flag 8.
		13	Program flag 4.
		14	Program flag 2.
		15	Program flag 1.
STS: Store Status (S) Register	S	7 thru 15	Same as LDS.

Table B-3. Type 2 Expanded Performance Module

Instruction/Word	A Register	
	Bit	Meaning
WTO0 thru WTO3: Load Segment Descriptor for Segments 0 thru 3	0 thru 8	Base address.
	9 thru 13	Maximum pages.
	14	Associated segment: 0 = exists. 1 = does not exist (size is zero in length).
	15	Write protect: 0 = writing into the segment permitted. 1 = writing into the segment prohibited.
LDM: Load DMA Base Address Register	0 thru 7	DMA base address.
Virtual Address (CPU generated)	0 and 1	Segment descriptor (0 thru 3).
	2 thru 6	Page number (0 thru 32).
	7 thru 15	Word number (0 thru 512).
RDS0: Read DMA Base Address Register and Status Indicators	0 thru 8	DMA base address.
	13	No-page error.
	14	Maximum-page error.
	15	Write-protect error.
RDS2: Read Address Causing Memory Protect Interrupt	0 thru 15	Memory Address.
RDS3: Read Address Sent Prior to Address Causing Memory Protect Interrupt	0 thru 15	Memory Address.
RDS4 thru RDS7: Read Segment Descriptors for Segments 0 thru 3	0 thru 15	Same as WTO0 thru WTO3.

Table B-4. High Capacity Removable Disc Controller (Sheet 1 of 2)

Instruction	A Register	
	Bit	Meaning
EDF SKC: Seek		2311 DISC:
	0 and 1	ZERO.
	2 thru 12	Binary track address.
		2312 DISC:
	0 thru 11	Binary track address.
EDF WRC: Write		2311 DISC:
	0 thru 1	ZERO.
	2 thru 15	Binary record address.
		2312 DISC:
	0 thru 15	Binary record address.
EDF RDC: Read	0 thru 15	Same as EDF WRC.
EDF SLC: Select Drive and Set Track Flags	6 and 7	Track flags.
	13 thru 15	Disc drive.
EDF FMT: Format Track	0 thru 15	Same as EDK SKC.
EDF RTD: Read Track Descriptor	0 thru 15	Same as EDF SKC.
WTO: Word Transfer Out	0 thru 15	Data to disc.
WTI: Word Transfer In	0 thru 15	Data from disc.
RDS MAJ: Read Major Status	0	Controller busy.
	1	Selected drive busy.
	2	Controller disconnected.
	3	Format protect.
	4	Drive 7 attention.
	5	Drive 6 attention.
	6	Drive 5 attention.

Table B-4. High Capacity Removable Disc Controller (Sheet 2 of 2)

Instruction	A Register	
	Bit	Meaning
	7	Drive 4 attention.
	8	Drive 3 attention.
	9	Drive 2 attention.
	10	Drive 1 attention.
	11	Drive 0 attention.
	12	Selected drive alert.
	13	Controller alert.
	14	Gated attention.
	15	Terminate.
RDS MIN: Read Minor Status	0	Selected drive off line.
	1	Selected drive unsafe.
	2	Selected seek incomplete.
	3	Drive selection error.
	6 and 7	Last flag bit.
	8	Write current sense.
	9	Selected pack change (2312 disc only).
	10	End of pack.
	11	Header verify error.
	12	Flag verify error.
	13	Data error.
	14	Rate error.
	15	Invalid address.
ICI: Interrogate Common Interrupts	0 thru 15	Common interrupt word.

Table B-5. Medium Capacity Disc Controller (Sheet 1 of 2)

Instruction	A Register	
	Bit	Meaning
EDF WRC: Fetch Control Words		
• Operation Control Word 1	0 thru 3	Op code. Specifies the operation to be performed on the disc files: X000 = read. X001 = write. X010 = verify. X011 = seek. X110 = read first halt sector. X111 = read second halt sector. *NOTE: If X is ONE the header check is inhibited.*
	4 thru 11	Number of records (sectors) to be operated on.
	14 and 15	Selects one of four drives for operation.
• Operation Control Word 2	0 thru 8	Desired cylinder for a seek operation.
		disc: 0 = removable. 1 = fixed.
	10	head: 0 = upper surface. 1 = lower surface.
	11 thru 15	Sector where a read or write operation is to begin.
• Operation Control Word 3	0 thru 15	Memory address of first data word transfer.
RDS ERR: Request Device Status (Error)	0*	Data error.
	1*	Address error.
	2*	Format error.
	3*	Program error.

*Indicates an error bit.

Table B-5. Medium Capacity Disc Controller (Sheet 2 of 2)

Instruction	A Register Bit	Meaning
	4*	Write protect error.
	5"	Timeout-error.
	6	Disc controller busy.
	7	Disc drive ready.
	8*	Rate error.
	9	Double track.
	10	Dual platter.
	11	Seek incomplete.
	12	Data transfer busy.
	13	Disc drive seeking.
	14 and 15	Disc drive address.
RDS GEN: Request Device Status (General)	0	System busy.
	1*	Memory over-run.
	2*	End of pack.
	3 thru 7	Selected soctor address.
	8	Disc drive 3 attention.
	9	Disc drive 2 attention.
	10	Disc drive 1 attention.
	11	Disc drive 0 attention.
	12	Selected disc drive alert.
	13	Disc controller alert.
	14	Gated attention.
	15	Terminate.
RDS HDR: Request Device Status (Last Record Header Used)	0 thru 7	Cylinder.
	8 thru 12	Sector.
	13	Platter (fixed or removable).
	14	Head (upper or lower surface).
ICI: Interrogate Common Interrupts	0 thru 15	Common interrupt word.

*Indicates an error bit.

Table B-6. Rotating Drum Memory Controller

Instruction	A Register	
	Bit	Meaning
EDF VFY: Verify		1004-S DRUM:
	3 and 4	Drum.
	5 thru 11	Track.
	12 thru 15	Sector.
		1016 DRUM:
	1 and 2	Drum.
	3 thru 11	Track.
	12 thru 15	Sector.
		1032 DRUM:
	1	Drum.
	2 thru 11	Track.
	12 thru 15	Sector.
		2032 DRUM:
	0	Drum.
	1 thru 10	Track.
	11 thru 15	Sector.
EDF WRC: Write Data Continuously	0 thru 15	Same as EDF VFY.
EDF RDC: Read Data Continuously	0 thru 15	Same as EDF VFY.
EDF ROS: Read One Sector	0 thru 15	Same as EDF VFY.
WTO: Word Transfer Out	0 thru 15	Data to drum.
WTI: Word Transfer In	0 thru 15	Data from drum.
RDS: Request Device Status	0	Not ready.
	1	Controller busy.
	2	Write protect violation.
	3	Illegal address.
	8 thru 12	Current sector of selected drum.

Table B-6. Rotating From Memory Controller (Sheet 2 of 2)

Instruction	A Register	
	Bit	Meaning
	13	Cyclic check error.
	14	Transfer timing error.
	15	Composite error including two or more of the errors identified by bits 0 thru 3, 13 and 14.
ICI: Interrogate Common Interrupts	0 thru 15	Common interrupt word.

Table B-7. Asynchronous Modem Multiplexer (Sheet 1 of 2)

Instruction	A Register	
	Bit	Meaning
EDF TMS: Terminal Set	0 and 1	Enable parity: 00 = No parity. 01 = Odd parity. 10 = Even parity.
	2 and 3	Character size: 00 = 8 bits. 01 = 7 bits. 10 = 6 bits. 11 = 5 bits.
	4 thru 7	Baud rate: 0000 = Nonstandard rate A. 0001 = Nonstandard rate B. 0010 = 75 baud. 0011 = 110 baud. 0100 = 134.5 baud. 0101 = 150 baud. 0110 = Nonstandard rate A. 0111 = 300 baud. 1000 = Nonstandard rate B. 1001 = 600 baud. 1010 = Nonstandard rate A. 1011 = Nonstandard rate B. 1100 = 1200 baud. 1101 = Nonstandard rate A. 1110 = 2400 baud. 1111 = 4800 baud.
	8 and 9	Stop bit size: 00 = 2 stop bits. 01 = 1.5/1.42 stop bits. 10 = 1 stop bit.

Table B-7. Asynchronous Modem Multiplexer (Sheet 2 of 2)

Instruction	A Register	
	Bit	Meaning
	10 thru 15	Line address.
EDF SCS: Special Conditions Set	0	Echoplex.
	1	Loop.
	2	Disable ring.
	3	Disable receive.
	4 thru 6	Common control.
	8 and 9	Special character set.
	10 thru 15	Line address.
EDF SLS: Select Line for Status	10 thru 15	Line Address.
WTO: Word Transfer Out	0	Word type: 0 = Normal data character. 1 = Special line condition.
	8 thru 15	Data character (bit 0 = 0).
	15	Condition (bit 0 = 1): 0 = Space hold. 1 = Mark hold.
WTI(A)*: Word Transfer In	0	I/O: 0 = Input to CPU. 1 = Output from CPU.
	10 thru 15	Line address.
WTI(B)*: Word Transfer In	0	Special character detect.
	1	Rate error.
	2	Parity error.
	3	Break candidate.
	8 thru 15	Data character.
RDS: Request Device Status	0	Carrier detect.
	1	Data set ready.
	2	Clear-to-send.
	3	Break indicator.
	4	Ring indicator.
	5 and 6	Common indicator.
	10 thru 15	Line address.
ICI: Interrogate Common Interrupts	0 thru 15	Common interrupt word.

*Letter in parentheses indicates device address

Table B-8. Asynchronous Communication Adapter (Sheet 1 of 2)

Instruction	A Register	
	Bit	Meaning
EDF TMS: Terminal Mode Set	2 and 3	Character size: 00 = 8 bits. 01 = 7 bits. 10 = 6 bits. 11 = 5 bits.
	4 thru 7	Data rate (in baud): 0000 = 300 thru 4800. } Nonstandard data rate 0001 = 75 to 300. } Nonstandard data rate 0110 = 25 to 75. } Nonstandard data rate 0010 = 75. } Standard data rate 0011 = 110. } Standard data rate 0100 = 134.5. } Standard data rate 0101 = 150. } Standard data rate 0111 = 300. } Standard data rate 1001 = 600. } Standard data rate 1100 = 1200. } Standard data rate 1110 = 2400. } Standard data rate 1111 = 4800. } Standard data rate
	8 and 9	Stop-bit size (in units): 00 = 2.00 01 = 1.50 thru 1.42 10 = 1.00
EDF SCS: Special Condition Set	0	Echoplex mode.
	1	Loop mode.
	2	Disable ring.
	3	Disable receive.
	4 thru 6	Common modem controls: X00* = modem control A. 0X0 = modem control B. 00X = modem control C.
	7	Enable DTR.
	8	Enable RTS.
	9	Select external clock.
EDF TST: Load Test Register	8	CTS signal.
	9	Common modem indicator B.
	10	Common modem indicator A.
	11	DSR signal.

*X indicates "either ONE or ZERO"

Table B-8. Asynchronous Communication Adapter (Sheet 2 of 2)

Instruction	A Register	
	Bit	Meaning
	12	Ring indicator.
	13	DCD signal.
	15	Deselect.
EDF SSC: Set Special Clock	4 thru 15	Preset value used to produce non-standard data rate ranging from 25 thru 300 baud.
WTO: Word Transfer Out	0	Special Transmitted Data Line condition.
	8 thru 15	Output character (when bit 0 is reset).
	15 only	Line condition (when bit 0 is set): 0 = space hold. 1 = mark hold.
WTI: Word Transfer In	0	Break indicator.
	1	Rate error indicator.
	3	Potential break indicator.
	8 thru 15	Input character.
RDS: Request Device Status	0	DCD indicator.
	1	DSR indicator.
	2	CTS indicator.
	3	Break indicator.
	4	Ring indicator.
	5	Common modem indicator A.
	6	Common modem indicator B.
ICI: Interrogate Common Interrupts	0 thru 15	Common interrupt word.

Table B-9. Synchronous Modem Multeplex (Sheet 1 of 2)

Instruction	A Register	
	Bit	Meaning
EDF TMS: Terminal Mode Set	1	Set request-to-send.
	2	1 = interrupt of data set ready transition.
	3	0 = Reset ring indicator bit. 1 = Set ring indicator bit.
	4 and 5	Protocol: 00 = No protocol detection. 01 = BSC test detection. 10 = BSC transparent detection. 11 = Alternate protocol detection.
	6	1 = Interrupt on SYNC character detection.
	7	1 = SYN character insertion/detection.
	8 thru 11	Operating mode: 0000 = Disconnect. 0001 = Transmit. 0010 = Receive. 0011 = Full-duplex. 0101 = Idle transmit. 0111 = Full-duplex with idle transmit. 1011 = Loop. 1111 = Loop with idle transmit.
	12 thru 15	Line number.
EDF SSL: Select Line	12 thru 15	Line number.
WTO: Word Transfer Out	2 thru 11	Data character.
	12 thru 15	Line number.
WTI(A)*: Word Transfer In	0	1 = Control character detected.
	12 thru 15	Line number.
WTI(B)*: Word Transfer In	0	1 = Control character detected.
	2 thru 11	Data character.
	12 thru 15	Line number.
RDS: Request Device Status	0	Protocol character received.
	1	DLE character stripped when in transparent mode.

*Letter in parentheses indicates device address

Table B-9. Synchronous Modem Multiplexer (Sheet 2 of 2)

Instruction	A Register	
	Bit	Meaning
	2	SYN character received.
	3	Parity error.
	4	Overflow.
	5	Underflow.
	6	Ring indicator.
	7	Line in character synchronization.
	8	Carrier detect.
	9	Data set ready.
	12 thru 15	Line number.
ICI: Interrogate Common Interrupts	0 thru 15	Common interrupt word.

Table B-10. Synchronous Communication Adapter (Sheet 1 of 5)

Instruction	A Register	
	Bit	Meaning
EDF SIM: Status Interrupt Mask	0	DCD interrupt.
	1	DSR interrupt.
	2	CTS interrupt.
	3	Ring indicator interrupt.
	4	Signal quality interrupt.
	5	Character sync interrupt.
	6	Transmit rate error interrupt.
	7	Receive rate error interrupt.
	8	Parity error interrupt.
	9	Sync error interrupt
	11 and 12	Block check interrupt. 01 = transmit. 10 = receive. 11 = both.
EDF TMS: Terminal Mode Set	0 and 1	Basic operating mode: 00 = BSC. 01 = general synchronous. 10 = start/stop.

Table B-10. Synchronous Communication Adapter (Sheet 2 of 5)

Instruction	A Register	
	Bit	Meaning
	2 and 3	Block check: 00 = none. 01 = CRC. 10 = LRC.
	4 and 5	Character lengths: 01 = six bits. 10 = seven bits. 11 = eight bits.
	6	Stop-bit size: 0 = one unit. 1 = two units.
	7	Sync character store: 0 = inhibit storing. 1 = store.
	8 and 9	Receive parity sense: 00 = odd. 01 = even. 1X*= none.
	10 and 11	Transmit parity sense: 00 = odd. 01 = even. 1X = none.
	12 thru 14	Data mode: X00 = idle. 001 = transmit. 010 = receive. 011 = full-duplex. 101 = idle transmit. 111 = full-duplex with idle transmit.
	15	Force DSR: 0 = normal operation. 1 = force DSR true.
EDF CIM: Control Character Interrupt Mask	0	Control character 0.
	1	Control character 1.
	2	Control character 2.

*X indicates "either ONE or ZERO"

Table B-10. Synchronous Communication Adapter (Sheet 3 of 5)

Instruction	A Register	
	Bit	Meaning
	3	Control character 3.
	4	Control character 4.
	5	Control character 5.
	6	Control character 6.
	7	Control character 7.
	8	Sync character.
EDF ACL: Alter Control Line	12	DTR true.
	13	RTS true.
	14	(Model 3071-01) data rate select. (Model 3071-02) modem test.
	15	New sync (Model 3071-01 only).
EDF TST: Test	0	DCD state.
	1	DSR state.
	2	CTS state.
	3	Ring indicator state.
	4	Signal quality state.
	5 and 6	Test clock: 00 = external. 01 = low. 10 = medium. 11 = high.
	7	Loop.
	8 and 9	DMA inhibit: 01 = output request (transmit). 10 = input request (receive). 11 = both.
EDF SCC: Store Control Character	0	Control character 0 (BSC = DLE).
	1	Control character 1 (BSC = STX).
	2	Control character 2 (BSC = ETX).
	3	Control character 3 (BSC = ETB).
	4	Control character 4 (BSC = ITB).
	5	Control character 5 (BSC = SOH).
	6	Control character 6 (BSC = ENQ).
	7	Control character 7

Table B-10. Synchronous Communication Adapter (Sheet 4 of 5)

Instruction	A Register	
	Bit	Meaning
	8	MSD: 0 = LSD of control character. 1 = MSD of control character.
	12 thru 15	Control character hexadecimal digit. Bit 15 is the least-significant bit of the value contained in bits 12 thru 15.
EDF SYN: Store Sync Character	8 thru 15	Sync character (bit 15 = first serial bit).
WTO OAD: Word Transfer Out, Output Address	0 thru 15	Output message segment memory starting address.
WTO OCT: Word Transfer Out, Output Count	0	Segment chain enable.
	1	Sync character insert.
	2	Transparent text message segment.
	4 thru 15	Output character count in two's complement form. Bit 4 is the most-significant bit of the value.
WTO IAD: Word Transfer Out, Input Address	0 thru 15	Input message segment memory starting address.
WTO ICT: Word Transfer Out, Input Count	4 thru 15	Input message segment character count.
WTI OAD: Word Transfer In, Output Address	0 thru 15	Same as WTO OAD.
WTI IAD: Word Transfer In, Input Address	0 thru 15	Same as WTO IAD.
RDS (0) and (1): Read Device Status	0	DCD state.
	1	DSR state.
	2	CTS state.
	3	Ring indicator state.
	4	Signal quality state.
	5	Character sync attained.

Table B-10. Synchronous Communication Adapter (Sheet 5 of 5)

Instruction	A Register	
	Bit	Meaning
	6	Transmit rate error.
	7	Receive rate error.
	8	Character flag; parity error, sync error or control character detected. The exact nature of the error is determined by bits 0 thru 2 of the data input word.
	9	Sync character detected.
	11 and 12	Block check character: XX1* = end of outgoing bcc. 10X = correct incoming bcc. 11X = incorrect incoming bcc.
	14 and 15	Segment end: 01 = transmit. 10 = receive. 11 = transmit and receive.
ICI: Interrogate Common Interrupts	0 thru 15	Common interrupt word.
Data Output Word	0	DLE control character indicator (BSC transparent text).
	1	Line hold (start/stop mode).
	8 thru 15	Data character (bit 15 = first serial bit).
Data Input Word	0	Control character.
	1	Parity error.
	2	Start/stop sync error.
	8 thru 15	Data character with unused bits reset (bit 15 = first serial bit).

*X indicates either ONE or ZERO

Table B-11. Automatic Calling Unit Multiplexer

Instruction	A Register	
	Bit	Meaning
EDF STP: Stop	12 thru 15	Stop ACU #0 thru #3 respectively.
EDF STR: Start	12 thru 15	Start ACU #0 thru #3 respectively.
EDF SWR: Inhibit PND	12 thru 15	Inhibit ACU #0 thru #3 respectively.
WTO: Output Dial Digit	8 thru 15	Dial digit.
	12 thru 15	ACU #0 thru #3 respectively.
WTI: Determine ACUs Requiring Service	0	Denotes error or status condition.
	12 thru 15	ACU #0 thru #3 respectively.
RDS: Read Status	0, 4, 8, 12	ACR for ACU #0 thru #3 respectively.
	1, 5, 9, 13	DSS for ACU #0 thru #3 respectively.
	2, 6, 10,14	DLO for ACU #0 thru #3 respectively.
	3, 7, 11,15	PWI for ACU #0 thru #3 respectively.

Table B-12. Block Check Unit

Instruction	A Register		
	Bit	Meaning	
EDF TMS: Terminal Mode Set	0	Mode: 0 = SCA. 1 = processor.	
EDF LDR: Load Register	0 thru 7	Second CRC character for output to communication controller.	Complete 16-bit CRC word.
	8 thru 15	First CRC character for output to communication controller.	
WTO: Word Transfer Out	8 thru 15	Data character (bit 15 = first serial bit).	
WTI: Word Transfer In	0 thru 7	Same as EDF LDR.	
RDS: Read Device Status	0	Error: 0 = Receive CRC Register equals zero. 1 = Receive CRC Register not equal to zero (CRC error).	
	1	Mode: 0 = SCA mode selected. 1 = processor mode selected.	

Table B-13. Communication Transfer Unit (Sheet 1 of 6)

Instruction/Word	A Register	
	Bit	Meaning
EDF WM1: Write One Word in Control Memory and EDF WM2: Write Two Words in Control Memory:		
• Transmit Control Word	0	Start/stop character (used with SMM only): 0 = eight-bit character. 1 = start/stop character.
	1 and 2	Block check character accumulation: 00 = none. 01 = longitudinal. 10 = cyclic. 11 = illegal.
	3	Transmission code: 0 = EBCDIC. 1 = ANSCII.
	4 thru 9	Code conversion table selection. These bits specify the portion of the code conversion memory that contains the code conversion table for the line selected.
	10	Byte position flag: 0 = left byte (data in bits 0 thru 7). 1 = right byte (data in bits 8 thru 15).
	11	Parity enable (significant only when bit 3 set): 0 = even. 1 = odd.
	12	SOH/STX character detection flag (significant only when bit 1 or 2 set).
	13	Zero parity: 0 = no affect. 1 = resets most-significant bit of output character.
	14	Transparent text indicator: 0 = other. 1 = transparent text.

Table B-13. Communication Transfer Unit (Sheet 2 of 6)

Instruction/Word	A Register	
	Bit	Meaning
	15	Data packing indicator: 0 = one character per memory word. 1 = two characters per memory word.
• Transmit Block Check Character Word		LONGITUDINAL:
	0	Bit always reset.
	1 thru 7	Block check character.
		CYCLIC:
	0 thru 7	First half of block check character.
	8 thru 15	Second half of block check character.
• Transmit Character Count Word	0	Bin (segment in processor memory) assigned: 0 = bin exhausted. 1 = bin assigned.
	1	Code conversion: 0 = disabled. 1 = enabled.
	2	Last segment or EDF SWR: 0 = meaningless. 1 = SMM: the last segment of a data block is being transmitted significant during transmission of transparent text only. AMM: instructs CTU to send EDF SWR to AMM when bit 0 is reset.
	3	Block check character indicator: 0 = data character being transmitted. 1 = LRC or CRC character being transmitted.
	4 thru 15	Character count in two's complement form.
• Transmit Memory Starting Address	0 thru 15	Starting address in memory of a segment that is to be transmitted.
• Receive Control Word	0 thru 10	Same as transmit control word bits 0 thru 10.

Table B-13. Communication Transfer Unit (Sheet 3 of 6)

Instruction/Word	A Register	
	Bit	Meaning
	11	Upper/lower case Baudot code flag: 0 = lower. 1 = upper.
	12	Same as transmit control word bit 12.
	13	ETB or ETX character detection flag.
	14	ITB character detection flag.
	15	CRC character received flag. Indicates that the first half of a CRC character has been received.
• Receive Block Check Character Word	0 thru 15	Same as the transmit block check character word.
• Receive Character Count Word	0 and 1	Same as transmit character count word bits 0 and 1.
	2	Parity indicator. 0 = even. 1 = odd.
	3	Data packing: 0 = one data character per 16-bit word. 1 = two data characters per 16-bit word.
	4 thru 15	Character count in two's complement form.
• Receive Memory Starting Address	0 thru 16	Starting address in memory of a new bin assigned for data to be received.
EDF RDM: Read One Word from Control Memory	0 thru 16	Same as any of the words stored using EDF WM1 or EDF WM2.
EDF WAM: Write Two Words in Mux-Address Memory		MUX-ADDRESS MEMORY WORD
	3	Multiplexer type. 0 = AMM. 1 = SMM.
	4 thru 9	Multiplexer A address.
	10 thru 15	Multiplexer B address.
	18 thru 27	Multiplexer starting address in the control memory.

Table B-13. Communication Transfer Unit (Sheet 4 of 6)

Instruction/Word	A Register	
	Bit	Meaning
EDF WCM: Write One Word in Code Conversion Memory		FIVE-BIT CONVERSION CHARACTER:
	0 thru 2	ZERO.
	3 thru 7	Conversion character.
		SIX-BIT CONVERSION CHARACTER:
	0 and 1	ZERO.
	2 thru 7	Conversion character.
		SEVEN-BIT CONVERSION CHARACTER:
	0	ZERO.
	1 thru 7	Conversion character.
		EIGHT-BIT CONVERSION CHARACTER:
	0 thru 7	Conversion character.
WTO: Word Transfer Out and WTI: Word Transfer I.	0 thru 7*	First character.
	8 thru 15*	Second character.
RDS: Request Device		WHEN STATUS WORD BIT 0 IS RESET:
	0	ZERO = interrupt generated for CTU.
	1	Mode: 0 = receive. 1 = transmit.
	2 thru 5	Status: 0000 = PIOB connected to I/O bus. Bits 6 thru 15 are meaningless. 0001 = PIOB ICI rejected. Bits 10 thru 15 are meaningless. 0010 = PIOB instruction rejected. Bits 10 thru 15 are meaningless. 0011 = BCC time (ETB/ETX). 0100 = end-of-segment. 0101 = data overrun. 0110 = EDF SWR sent to AMM. 0111 = BCC time (ITB). 1000 = SMM control character. 1001 = good BCC (ETB/ETX).

*When data packing is used

Table B-13. Communication Transfer Unit (Sheet 5 of 6)

Instruction/Word	A Register	
	Bit	Meaning
		1010 = SMM control character and PIOB instruction rejected. 1011 = SMM control character and BCC time. 1100 = SMM control character and end-of-segment. 1101 = SMM control character and data overrun. 1110 = bad BCC (ITB). 1111 = bad BCC (ETB/ETX).
	6 thru 9	Multiplexer number.
	10 thru 15	Line number.
		WHEN STATUS WORD BIT 0 IS SET:
	0	ONE = interrupt generated for AMM.
	2	Potential break.
	3	Parity error.
	4	Rate error.
	5	Special character detected.
	6 thru 9	Multiplexer number.
	10 thru 15	Line number.
ICI: Interrogate Common Interrupts	0 thru 15	Common interrupt word.
EDF WIR: Write in Interrupt Register (CTUVM)	0 thru 15	A ONE in any bit position (0 thru 15) causes an interrupt condition on the line assigned to that bit position.
EDF WAR: Write in Mux-Address Register (CTUVM)	4 thru 9	Multiplexer A device address.
	10 thru 15	Multiplexer B device address.
EDF WRA: Write in Response Register A (CTUVM)		AMM:
	0	I/O: 0 = input to CPU. 1 = output from CPU.
	10 thru 15	Line address.

Table B-13. Communication Transfer Unit (Sheet 6 of 6)

Instruction/Word	A Register	
	Bit	Meaning
		SMM:
	0	Control character detected.
	12 thru 15	Line number.
EDF WRB: Write in Response Register B (CTUVM)		AMM:
	0	Special character detect.
	1	Rate error.
	2	Parity error.
	3	Break candidate.
	8 thru 15	Data character.
		SMM:
	0	Control character detected.
	2 thru 11	Data character.
	12 thru 15	Line number.
EDF WRC: Write in Response Register C (CTUVM)	0 thru 15	AMM or SMM common interrupt word.
EDF WCR: Write in Control Register (CTUVM)	8	Enable PIOB WTI(A) decoder.
	9	Enable PIOB WTI(B) decoder.
	10	Enable PIOB WTO(A) decoder.
	11	Enable PIOB ICI(A) decoder.
	12	Enable PIOB EDF SWR(A) decoder.
	13	PIOB interrupt cycle: 0 = multiple. 1 = single.
	14	Reset CTUVM control logic.
	15	Spare.
RDS: Request Device Status (CTUVM)	0 thru 15	Data present on the PIOB DDB00 thru DDB15 lines, during execution of WTO(A).
ICI: Interrogate Common Interrupt (CTUVM)	0 thru 15	Common interrupt word.

Table B-14. System Control Unit

Instruction	A Register	
	Bit	Meaning
EDF(1): Connect Switch to Issuing CPU	0 thru 15	Switches 0 thru 15 respectively: 1 = transfer control to processor issuing instruction.
EDF(2): Disconnect Switch from Issuing CPU	0 thru 15	Switches 0 thru 15 respectively: 1 = transfer control of switched element to neutral position and generate interrupt.
RDS(1): Read Status of Control Flip-Flop Units (Switches connected to issuing CPU)	0 thru 15	State of control flip-flops: 0 = either other processor or neither processor has control. 1 = processor issuing instruction has control.
RDS(2): Read Status of Control Flip-Flop Units (Switches connected to other CPU)	0 thru 15	State of control flip-flops: 0 = either processor issuing instruction has control of switched element or switch is in center position. 1 = other processor has control of switched element.
RDS(3): Read Status of Control Flip-Flop Units and Reset Interrupt (Switches connected to other CPU)	0 thru 15	Same as RDS(2).
RDS(4): Read Status Manual Toggle Switches	0 thru 15	Status of toggle switches: 0 = toggle switch in neutral position. 1 = toggle switch manually moved from neutral position.
RDS(5): Read Power Block Status	0	Interrupt button pressed.
	1	0 = system 1. 1 = system 2.
	2 thru 14	Status of power blocks 0 thru 14, respectively: 0 = corresponding power block off. 1 corresponding power block energized.
ICI: Interrogate Common Interrupts	0 thru 15	Common interrupt word.

Table B-15. Terminal Control Channel Interface Unit (Sheet 1 of 3)

Instruction	A Register	
	Bit	Meaning
EDF WRC: Write Continuously	11	Burst mode.
	15	Byte transfer mode.
EDF RDC: Read Continuously	10	Read immediate.
	11	Burst mode.
	13	Inhibit INTC.
	14	Character detection enabled.
	15	Byte transfer mode.
EDF LIN: Line	15	0 = put TCIU off-line to channel. 1 = put TCIU on-line to channel.
EDF WAS: Write Address	0	Channel burst mode from poll sequence.
	4 thru 7	Number of bytes per data transfer sequence.
	8 thru 15	Line address.
EDF BSY: Busy	15	0 = Reset CU busy FF. 1 = Set CU busy FF.
WTO DTA: Data Out	0 thru 7	Data byte number 1 if in word mode.
	8 thru 15	Data byte number 1 if in byte mode. Data byte number 2 if in word mode.
WTO INS: Initial Status	0	Channel burst mode from initial selection sequence.
	6	Abort status request or data transfer request to channel.
	7	0 = clear CU busy FF.
	8 thru 15	Initial status.
WTO CHR: Character Detection	9 thru 15	Character to be detected.
WTO STS: Noninitial Status	0	1 = status stacked on previous attempt.
	8 thru 15	Noninitial status.
WTO BUS: Bus Out	7	Test bus out parity.
	8 thru 15	Test bus out 0 thru 7.
WTO TAG: Tag Out	7	Test clock out.
	8	Test suppress out.

Table B-15. Terminal Control Channel Interface Unit (Sheet 2 of 3)

Instruction	A Register	
	Bit	Meaning
	9	Test select out.
	10	Test hold out.
	11	Test operational out.
	12	Test metering out.
	13	Test command out.
	14	Test address out.
	15	Test service out.
WTI DTA: Data In	0 thru 7	Data byte number 1 if in word mode.
	8 thru 15	Data byte number 1 if in byte mode. Data byte number 2 if in word mode.
WTI BYT: Byte Count	12 thru 15	Buffer memory byte counter.
WTI FAD: FEP-Initiated Line Address	8 thru 15	FEP-initiated line address.
WTI ISA: Initial Selection Line Address	8 thru 15	Initial selection line address.
WTI ISC: Initial Selection Command	0	Command not yet received from channel.
	8 thru 15	Initial selection command.
WTI BUS: Bus In	7	Test bus in parity.
	8 thru 15	Test bus in 0 thru 7.
WTI TAG: Tag In	9	Test propagated select out.
	10	Test request in.
	11	Test operational in.
	12	Test metering in.
	13	Test status in.
	14	Test address in.
	15	Test service in.
RDS RES: Read Resettable Device Status	0	Noninitial status accepted by channel.
	1	Noninitial status stacked by channel.
	2	Initial status stacked by channel.

Table B-15. Terminal Control Channel Interface Unit (Sheet 3 of 3)

Instruction	A Register	
	Bit	Meaning
	3	Data stop.
	4	Interface disconnect during initial selection.
	5	Interface disconnect during poll sequence.
	6	Initial status accepted by channel.
	7	Selective reset during poll sequence.
	8	Selective reset during initial selection.
	9	System reset from channel.
	10	Data parity error.
	11	On-line/off-line transition requested.
	12	Command chaining.
	13	Character detected.
	14	Channel-initiated channel burst mode.
RDS NRS: Read Nonresettable	0	TCIU busy.
	1	TCIU on-line to channel.
	2	CU busy.
	3	TCIU in channel-burst mode.
RDS SEL: Read Initial Selection Status	0	Noninitial status accepted by channel.
	1	Noninitial status stacked by channel.
	2	Initial status stacked by channel.
	3	Data stop.
	4	Interface disconnect during initial selection.
	5	Interface disconnect during poll sequence.
	6	Initial status accepted by channel.
	7	Selective reset during poll sequence.
	8	Selective reset during initial selection.
	9	System reset from channel.
	10	Data parity error.
	11	On-line/off-line transition requested.
	12	Command chaining.
	13	Character detected.
	14	Channel-initiated channel-burst mode.

Table B-16. Tape Unit Channel Interface Unit (Sheet 1 of 3)

Instruction	A Register	
	Bit	Meaning
EDF WRC: Write Continuously	11	Burst mode.
	15	Byte transfer mode.
EDF RDC: Read Continuously	10	Read immediate.
	11	Burst mode.
	13	Inhibit INTC.
	14	Character detection enabled.
	15	Byte transfer mode.
EDF LIN: Line	15	0 = put TCIU off-line to channel. 1 = put TCIU on-line to channel.
EDF WAS: Write Address	0	Channel burst mode from poll sequence.
	4 thru 7	Number of bytes per data transfer sequence.
	8 thru 15	Line address.
EDF BSY: Busy	15	0 = reset CU busy FF. 1 = set CU busy FF.
WTO DTA: Data Out	0 thru 7	Data byte number 1 if in word mode.
	8 thru 15	Data byte number 1 if in byte mode. Data byte number 2 if in word mode.
WTO CHR: Character Detection	9 thru 15	Character to be detected.
STO STS: Noninitial Status.	0	1 = status stacked on previous attempt.
	8 thru 15	Noninitial status.
WTO BUS: Bus Out	7	Test bus out parity.
	8 thru 15	Test bus out 0 thru 7.
WTO TAG: Tag Out	7	Test clock out.
	8	Test suppress out.
	9	Test select out.
	10	Test hold out.
	11	Test operational out.
	12	Test metering out.
	13	Test command out.
	14	Test address out.
	15	Test service out.

Table B-16. Tape Unit Channel Interface Unit (Sheet 2 of 3)

Instruction	A Register	
	Bit	Meaning
WTI DTA: Data In	0 thru 7	Data byte number 1 if in word mode.
	8 thru 15	Data byte number 1 if in byte mode. Data byte number 2 if in word mode.
WTI BYT: Byte Count	12 thru 15	Buffer memory byte counter.
WTI FAD: FEP-Initiated Line Address	8 thru 15	FEP-initiated line address.
WTI ISA: Initial Selection Line Address	8 thru 15	Initial selection line address.
WTI ISC: Initial Selection Command	0	Command not yet received from channel.
	8 thru 15	Initial selection command.
WTI BUS: Bus In	7	Test bus in parity.
	8 thru 15	Test bus in 0 thru 7.
WTI TAG: Tag In	9	Test propagated select out.
	10	Test request in.
	11	Test operational in.
	12	Test metering in.
	13	Test status in.
	14	Test address in.
	15	Test service in.
RDS RES: Read Resettable Device Status	0	Noninitial status accepted by channel.
	1	Noninitial status stacked by channel.
	2	Initial status stacked by channel.
	3	Data stop.
	4	Interface disconnect during initial selection.
	5	Interface disconnect during poll sequence.
	6	Initial status accepted by channel.
	7	Selective reset during poll sequence.

Table B-16. Tape Unit Channel Interface Unit (Sheet 3 of 3)

Instruction	A Register	
	Bit	Meaning
	8	Selective reset during initial selection.
	9	System reset from channel.
	10	Data parity error.
	11	On-line/off-line transition requested.
	12	Command chaining.
	13	Character detected.
	14	Channel-initiated channel burst mode.
RDS NRS: Read Nonresettable	0	TCIU busy.
	1	TCIU on-line to channel.
	2	CU busy.
	3	TCIU in channel-burst mode.
RDS SEL: Read Initial Selection Status	0	Noninitial status accepted by channel.
	1	Noninitial status stacked by channel.
	2	Initial status stacked by channel.
	3	Data stop.
	4	Interface disconnect during initial selection
	5	Interface disconnect during poll sequence.
	6	Initial status accepted by channel.
	7	Selective reset during poll sequence.
	8	Selective reset during initial selection.
	9	System reset from channel.
	10	Data parity error.
	11	On-line/off-line transition requested.
	12	Command chaining.
	13	Character detected.
	14	Channel-initiated channel-burst mode.
ICI: Interrogate Common Interrupts	0 thru 15	Common interrupt word.

Table B-17. Input/Output Processor

Instruction	A Register	
	Bit	Meaning
EDF RAI: Reset Bus A Interrupt	8 thru 11	ONE resets IOP generated interrupts by resetting corresponding overflow flip-flops 8 thru 11.
EDF SIF: Set High-Rate Interrupt Flags	8 thru 11	ONE sets high-rate interrupt flags corresponding to Bus B interrupts 8 thru 11.
EDF RIF: Reset High-Rate Interrupt Flags	8 thru 11	ONE resets high-rate interrupt flags corresponding to Bus B interrupts 8 thru 11.
EDF SMR: Set Mask Register	8 thru 11	ONE sets Mask Register bits corresponding to Bus B interrupts 8 thru 11.
EDF RMR: Reset Mask Register	8 thru 11	ONE resets Mask Register bits corresponding to Bus B interrupts 8 thru 11.
WTO ADR: Transfer Out Address - Channel 0 thru 3		WORD TRANSFER:
	0 thru 15	Beginning memory address of high-rate interrupts 8 thru 11.
		BYTE TRANSFER:
	0 thru 14	Beginning memory address of high-rate interrupts 8 thru 11.
WTO CTL: Transfer Out Control Word - Channel 0 thru 3	0	0 = I/O write, memory read. 1 = I/O read, memory write.
	1	0 = byte transfer. 1 = word transfer.
	2 thru 15	Word/byte count in two's complement form.
WTI ADR: Transfer In Address - Channel 0 thru 3	0 thru 15	Same as WTO ADR.
WTI CTL: Transfer In Control Word - Channel 0 thru 3	0 thru 15	Same as WTO CTL.
RDS: Request Device Status	0 thru 3	State of high-rate interrupt flags 8 thru 11.
	8 thru 11	State of Mask Register bits 8 thru 11.
ICI: Interrogate Common Interrupts	0 thru 15	Common interrupt word.

Table B-18. High Speed Paper Tape Reader/Punch Controller

Instruction	A Register	
	Bit	Meaning
WTO: Word Transfer Out	0 thru 7	Data output to paper tape punch.
WTI: Word Transfer In	8 thru 15	Data input from paper tape reader.
RDS0: Read Reader Status	0	Not ready.
	1	Ready.
RDS1: Read Punch Status	0	Not ready.
	1	Ready.
ICI: Interrogate Common Interrupts	0 thru 15	Common interrupt word.

Table B-19. Card Reader/Line Printer Controller (Sheet 1 of 2)

Instruction	A Register	
	Bit	Meaning
EDF SPO: Set Printer Operations		CDC PRINTER:
	6	Deselect printer.
	7	Enable compact data mode.
	8	Enable print complete interrupt.
	9	Enable automatic TOF.
		DPC PRINTER:
	10 thru 15	000000 = no advance. 000001 = advance one line. 000010 = advance two lines. thru thru 110111 = advance 55 lines. 111000 = advance to VFU Channel 1 (TOF). 111001 = advance to VFU Channel 2 thru thru 111110 = advance to VFU Channel 7. 111111 = advance to VFU Channel 8 bottom of form.
EDF API: Advance Paper Immediately	10 thru 15	Same as EDF SPO.

Table B-19. Card Reader/Line Printer Controller (Sheet 2 of 2)

Instruction	A Register	
	Bit	Meaning
WTO: Word Transfer Out	2 thru 7	Data character 1.
	10 thru 15	Data character 2.
RDS: Request Device Status	0	Not ready. Controller is in print or paper advance cycle, or data printer line printer is not ready.
	1	Controller is in print or paper advance cycle.
	2	Printer out of forms.
	3	Paper at VFU Channel 2.
	4	Printer not on-line.
	5	Printer not ready.
	6	Printer not able to accept data. Bit is valid only after EDF WRC.
ICI: Interrogate Common Interrupts	0 thru 15	Common interrupt word.

Table B-20. Standard Card Punch Controller

Instruction	A Register	
	Bit	Meaning
WTO: Word Transfer Out	0 thru 15	Data to punch.
RDS: Request Device Status	0	Punch busy. A punch cycle is in progress.
	1	Card buffer memory full.
	2	Controller terminate (interrupt flip-flop).
	13	Punch fault. An abnormal condition exists in the punch.
	14	Hole check error. The punch has detected a misspunched card.
	15	Any error. Inclusive OR of bits 13 and 14.
ICI: Interrogate Common Interrupts	0 thru 15	Common interrupt word.

Table B-21. Universal Magnetic Tape Controller (Sheet 1 of 2)

Instruction	A Register	
	Bit	Meaning
EDF WRC: Fetch Control Words		
• Operation Control Word CSA	0 thru 3	Op code: Op Code — Tape Transport Command 0000 — Read Forward (RDF). 0001 — Write Forward (WRT). 0010 — File Mark Search Forward (FSF). 0011 — Write File Mark (WFM). 0100 — Read Reverse (RDR). 0101 — Erase (ERS). 0110 — File Mark Search Reverse (FSR). 0111 — Rewind (REW). 1000 — Select Transport (SEL). 1001 — Off Line (OFF). 1010 thru 1111 — Illegal Codes.
	13	Parity sense: 0 = even. 1 = odd.
	14 and 15	Tape transport number: 00 = tape transport no. 0. 01 = tape transport no. 1. 10 = tape transport no. 2. 11 = tape transport no. 3.
• Operation Control Word CSA+1	4 thru 15	Byte Count.
• Operation Control Word CSA+2	0 thru 15	Starting address of the data buffer.
RDSO: Read Primary Device Status	0	Controller busy.
	1	Tape transport not ready. This bit is reset only when all the following conditions exist: • All interlocks are made. • Initial load or rewind sequence is complete and tape is at the load point. • Tape transport is on-line. • Tape transport is not rewinding.

Table B-21. Universal Magnetic Tape Controller (Sheet 2 of 2)

Instruction	A Register	
	Bit	Meaning
	2	Tape transport off-line. When this bit is set, the tape transport is under local control and cannot be operated remotely.
	3	Write enable. Power is on and a reel of tape with a write enable ring is mounted on the tape transport.
	4	Tape transport rewinding.
	5	Beginning-of-tape.
	6	End-of-tape.
	7	File mark read.
	8	Hard error. One of the following error conditions has been detected: o Parity error. o LRC error. o CRC error. o Format error (NRZI formatter only): o More than two CRC characters. o More than two LRC characters.
	9	Corrected error (PE formatter only).
	10	Identification (PE formatter only). The identification burst has been detected.
	11	Phase encoded. The selected tape transport is configured for PE data transfers.
	12	Rate error detected.
	13	Tape transport head type: 0 = nine track. 1 = seven track.
	14 and 15	Tape transport address: 00 = tape transport no. 0. 01 = tape transport no. 1. 10 = tape transport no. 2. 11 = tape transport no. 3.
RDS1: Read Secondary Device Status	0	Invalid command.
	1	Odd number of bytes read.
	4 thru 15	Byte count. These bits contain the contents of the Byte Counter after a read, write or file mark search operation has been completed.
ICI: Interrogate Common Interrupts	0 thru 15	Common interrupt word.

Table B-22. Utility Control and Distributor and Utility Controller

Instruction	A Register	
	Bit	Meaning
EDF WOC: Write One Character	0 thru 7	Data to TTY.
WTI: Word Transfer In	8 thru 15	Data from the TTY.
RDS: Read Device Status	8	TINT+. TTY controller interrupt.
	9	ETINP+: 0 = noninterrupt mode. 1 = interrupt mode.
ICI: Interrogate Common Interrupts	0 thru 15	Common interrupt word.

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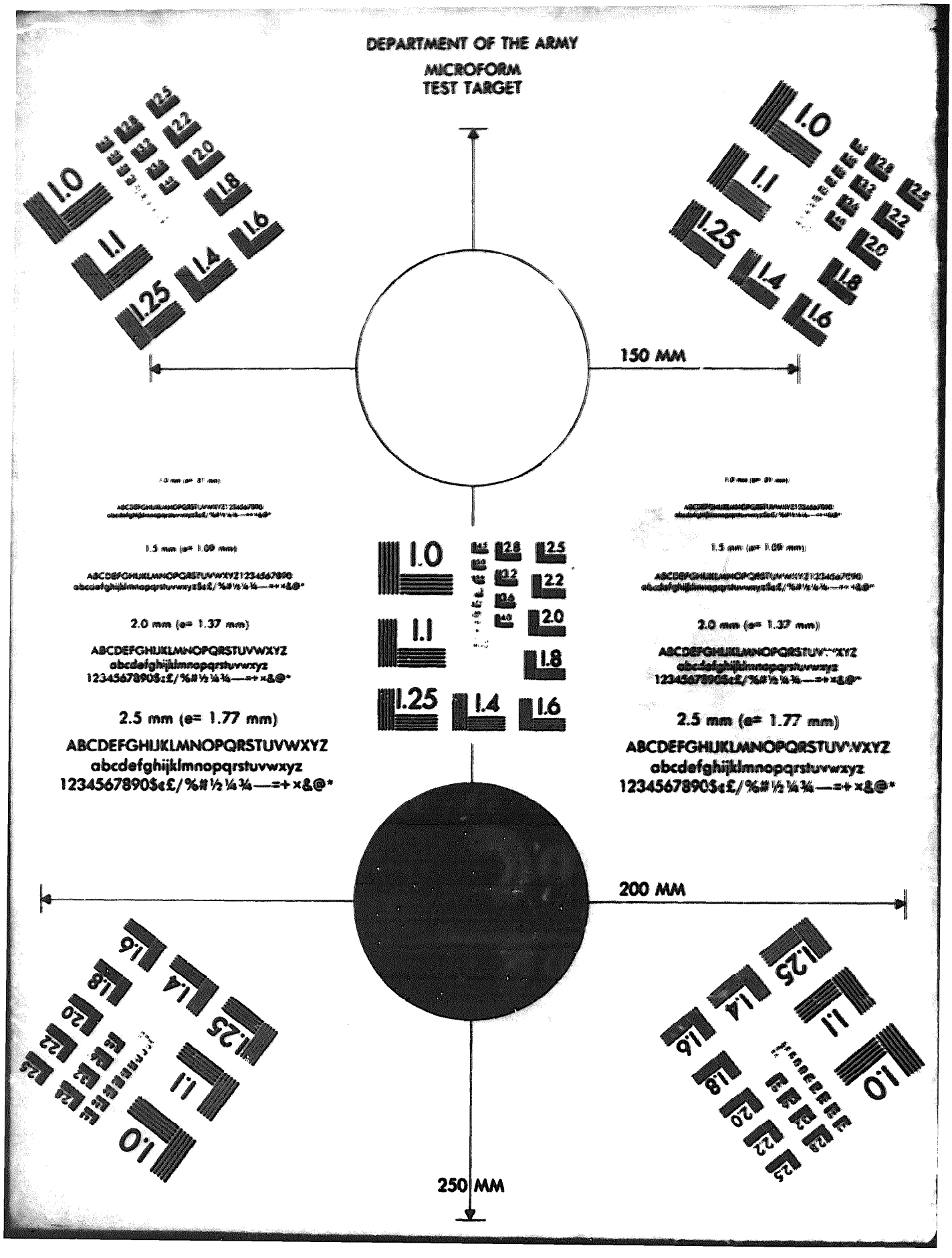
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